GEORGIA INSTITUTE OF TECHNOLOGY — OFFICE OF CONTRACT ADMINISTRATION

PROJECT ADMINISTRATION DATA SHEET

[x] ORIGINAL [ ] REVISION NO. _____

Project No. A-3459 GTRI/~~GTE~~ DATE 1/27/83

Project Director: H. M. Harris ~~School~~/Lab EML/PSD

Sponsor: Hughes Aircraft Co.

Type Agreement: P. O. S8-879406-LPY

Award Period: From 1/3/83 To ~~1/9/84~~ 3-9-84 (Performance) 1/9/84 (Reports)

Sponsor Amount: Total Estimated: $ 99,937 Funded: $ 99,937

Cost Sharing Amount: $ _____ Cost Sharing No: _____

Title: Low Noise GaAs FET-Phase II

ADMINISTRATIVE DATA

OCA Contact Frank Huff

1) Sponsor Technical Contact:

J. W. Kinney
Bldg. S12, M/S W323
Hughes Aircraft Co.
P. O. Box 92919-Airport Station
Los Angeles, CA 90009

(213) 648-8693

2) Sponsor Admin/Contractual Matters:

J. W. Kinney
Bldg. S12, M/S W323
Hughes Aircraft Co.
P. O. Box 92919-Airport Station
Los Angeles, CA 90009

(213) 648-8693

Defense Priority Rating: NA

Military Security Classification: _____
(or) Company/Industrial Proprietary: _____

RESTRICTIONS

See Attached _____ Supplemental Information Sheet for Additional Requirements.

Travel: Foreign travel must have prior approval — Contact OCA in each case. Domestic travel requires sponsor approval where total will exceed greater of $500 or 125% of approved proposal budget category.

Equipment: Title vests with none proposed

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GEORGIA INSTITUTE OF TECHNOLOGY OFFICE OF CONTRACT ADMINISTRATION

SPONSORED PROJECT TERMINATION/CLOSEOUT SHEET

Date June 11, 1984

roject No. A-3459 ~~School~~/Lab EML/PSD

ncludes Subproject No.(s)

roject Director(s) H. M. Harris GTRI / ~~GIT~~

ponsor Hughes Aircraft Co.

tle Low Noise GaAs FET - Phase II

fective Completion Date: 3/9/84 (Performance) 3/9/84 (Reports)

rant/Contract Closeout Actions Remaining:

- [ ] None
- [x] Final Invoice or Final Fiscal Report
- [ ] Closing Documents
- [ ] Final Report of Inventions
- [ ] Govt. Property Inventory & Related Certificate
- [ ] Classified Material Certificate
- [ ] Other

ntinues Project No. Continued by Project No.

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rm OCA 60:1028

Del No. 1

Status Report 1

LOW NOISE GaAs FET - PHASE II

Contract period covered
3 January 1983 through 31 January 1983
P.O. No. S8-879406-LPY

A-3459

Submitted to
Hughes Aircraft Company
El Segundo, California 90245

by
Physical Sciences Division
Electromagnetics Laboratory
Engineering Experiment Station
Georgia Institute of Technology
Atlanta, Georgia 30332

Contracting through
Georgia Tech Research Institute
Georgia Institute of Technology
Atlanta, Georgia 30332

February 7, 1983

INTRODUCTION

This report describes the work performed on the program during the month of January. Notice of contract award was obtained near the end of the month resulting in a technical effort of approximately one week. CAD facilities at Georgia Tech were completed in December and familiarization and preliminary mask design were initiated. Plans to modify the E-beam evaporation system were also formalized during this abbreviated period. Personnel to be utilized on this effort include Mike Harris, Jerry Hill and Lee Wiederspahn (Graduate Student). Other staff members will be used as the need and their expertise dictate.

TECHNICAL EFFORT

Contract Item 2 - Define Mask Set

The RFIC mask set employed in phase I is well suited for providing a variety of microwave circuit elements (filters, amplifiers and couplers) using a mature fabrication process. However, for process development and FET evaluation, a mask set having more discrete devices per unit area is desirable.

As a result of discussions with Hughes during the program review of phase I, several process related features, necessary for state-of-the-art devices, were emphasized. Multiple gate feeds are necessary to reduce gate resistance. The use of multiple gate feeds necessitates a crossover method to connect source elements. Dielectric layer isolation and air bridge

technology are two methods of providing crossovers. Provisions for air bridges are being included in this mask design.

High performance devices require narrow gate lengths. Devices with gate lengths of 1.0, 0.75, 0.5 and 0.25 μm will be attempted with the proposed mask set. However, mask makers contacted to date will not guarantee the 0.25 μm dimension.

Crystalline orientation of the FETs was another consideration. FETs rotated 90° from the standard device direction will be included to assess the possible crystallographic effects.

In addition to multiple gate feeds, thick gates (mushroom structure) are used to reduce gate resistance. In order provide for gate recess and thick gates, two gate masks are proposed. A wide gate mask will be used for initial recess. Final gate recess and deposited narrow gate will be performed using a narrow gate mask. Remasking with the wide gate mask and gold electroplating will complete the gate process.

In addition to the various FET geometries, diagnostic patterns are also planned.[1] Proposed test patterns include:

- active layer CV
- isolation test
- Greek cross for mobility measurement
- 1 μm FET
- ohmic contact test pattern
- gate resistance pattern
- Fat FET[2]

Preliminary design of this mask set is currently in progress using a CALMA GDS-II system. The attached plot is one unit cell having the approximate dimensions of 120 by 140 mils and consisting of the diagnostic pattern discussed above plus:

Unbridged Devices

Qt	Width (μm)	Length (μm)
8	100	(2 each length)
8	200	(2 each length)
4	200	(1 each length) oriented 90°
11	300	(3 each 1.0, 0.75,0.5) (2 each .25)

Bridged Devices

Qt	Width (μm)	Length (μm)
8	100	(2 each length)
6	200	(2 each 1.0,0.75,0.5)
3	200	(1 each 1.0,0.75,0.5) oriented 90°
9	300	(3 each 1.0,0.75,0.5)

Design rules established for this mask set are basically the same as the RFIC design rules. Drain to source spacing (ohmic) is

specified as 3 times the gate length. Having the possibility of 57 FETs per unit cell, process development much should be easier.

Contract Item 3 - Modify E-beam System

System disassembly has been performed to determine the best approach to increase the source to substrate spacing. Modification is rather difficult due to the mechanism used to position the multiple crucible hearth. Determination of the maximum substrate temperature obtained with the present configuration is under way. A thermistor sensor is being assembled and calibrated. Connection of the sensor to the system will be made using the present thickness monitor contacts.

PLANS FOR NEXT MONTH

- Continue mask design effort
- Continue E-beam modification
- Order GaAs Wafers
- Measure gate diode forward characteristics on phase I FETs if available

REFERENCES

1. A. A. Immorlica, Jr. etal. "A Diagnostic Pattern for GaAs FET Material Development and Process Monitoring," IEEE Trans. Electron Devices, Vol. Ed.-27. pp. 2285-2291.

2. P. A. Pucel, C. F. Krumm, "Simple Method of Measuring Drift-Mobility Profiles in Thin Semiconductor Films," Electronic Letters, Vol. 12 13 May 1976.

Del No. 2

Status Report 2

LOW NOISE GaAs FET - PHASE II

Contract period covered
1 February 1983 through 28 February 1983
P.O. No. S8-879406-LPY

A-3459

Submitted to
Hughes Aircraft Company
El Segundo, California 90245

by
Physical Sciences Division
Electromagnetics Laboratory
Engineering Experiment Station
Georgia Institute of Technology
Atlanta, Georgia 30332

Contacting through
Georgia Tech Research Institute
Georgia Institute of Technology
Atlanta, Georgia 30332

March 10, 1983

INTRODUCTION

This report describes the work performed on the program during the month of February. CAD of the mask set is continuing. Modification of the electron beam deposition system has been initiated. GaAs material requirements have been determined and wafers have been ordered. Schottky gate diode characteristics have been measured on FETs fabricated during phase I.

TECHNICAL EFFORT

Contract Item 2 - Define Mask Set

Preliminary design of the mask set discussed in the previous monthly report is continuing. Proposed mask levels and their order of use are as follows:

LEVEL #	DESCRIPTION
1	Ohmic Contact
2	Mesa
3	Wide Gate
4	Narrow Gate and Pads
5	Electroplate
6	Vias for Air Bridge
7	Air Bridge

Attached are plots which show each mask level for a 300 micron bridged FET and the diagnostic structure. Levels 6 and 7 are on the same plot for brevity. At the present time, several changes have been suggested to improve fabrication, identification, and performance. These proposed changes include:

- o deleting source interconnect metallization on level 1 (an extraneous active region and a more difficult air bridge process result otherwise)
- o add pads for via contact on level 5
- o modify geometries to accomodate a gate air bridge interconnect metallization of 20 microns in width
- o form separate mesas on each side of the gate feed lines (source and drain ohmic contact pattern would be identical)
- o make the gate feed lines at least 5 microns wide
- o pattern a 500 micron long ruler, having 50 micron subdivisions, and locate it below the diagnostic structure (ohmic level)
- o move the source pads closer to the FET (eliminating the stem from the triangular pad)
- o label pads on the diagnostic structure
- o pattern date (month/year) in the cell (ohmic level).

These changes along with any other changes which may be required as a result of the review of the attached plots will made during the next 1 1/2 months. Plans are to have the mask set design ready for formal review by the end of April.

Contract Item 3 - Modify E-beam System

In order to determine the maximum substrate temperature obtained with the existing system, a thermistor sensor was calibrated and mounted on a GaAs wafer. The assembly was spray

coated with AZ1350J photoresist to simulate actual deposition conditions as closely as possible.

Heating tests, performed with the Pt source at power levels below the Pt evaporation level, disclosed the following relationships:

E-beam Power (kW)	Pt. Temp. (°C)	Time (sec)	Substrate Temp. (°C)
.1	1454	10	115
.3	1554	10	160
.5	1660	10	190

Notes: Pt temperature measured with an optical pyrometer. Substrate temperature allowed to cool to <30 °C prior to the 10 sec exposure.

As seen from these results, excessive heating occurs at power levels below that required to deposit Ti (typically .6 kW).

Actual deposition of Ti was next performed by first heating the Ti at idle power for 75 sec. and then .6 kW. The data below show the results of the deposition run.

Power (kW)	Ti Temp. (P °C)	Time (sec)	Substrate Temp. (P °C)
Idle	1132	75	125
.6	1443	10	165
.6	1443	20	210

Notes: Two minutes of cooling between cycles.

Substrate cooled to <40°C between cycles.

Based on the substrate temperatures noted during the deposition run, it was clear that a significant increase in the source to substrate distance was necessary. Due to the relatively fixed focal length of the E-gun, simply lowering the hearth with respect to the substrate holder and E-gun was not considered feasible. Modification of the substrate holder, emission opening and shutter were performed. Tests are in progress to evaluate these modifications. Completion of this task appears to be possible by the scheduled data.

Contract Item 4 - Procure GaAs Epitaxial Material

GaAs epitaxial material specifications have been prepared based on phase I efforts and subsequent computer simulation. These specifications are listed below:

Substrate

2" diameter Bridgeman

Semi - insulating

Buffer Layer

conc. $< 5 \times 10^{14}$ cm^{-3}

thickness > 2.5 microns

Active Layer

conc. $= 1.8 \pm .2 \times 10^{17}$ cm^{-3}

thickness = $0.15 \pm .05$ microns

A purchase order for material meeting these specifications has been placed with Raytheon. Three wafers were ordered under a

blanket P.O. so that one wafer can be evaluated prior to delivery of the other wafers. Receipt of the first wafer is expected by mid-April.

Schottky Gate Evaluation

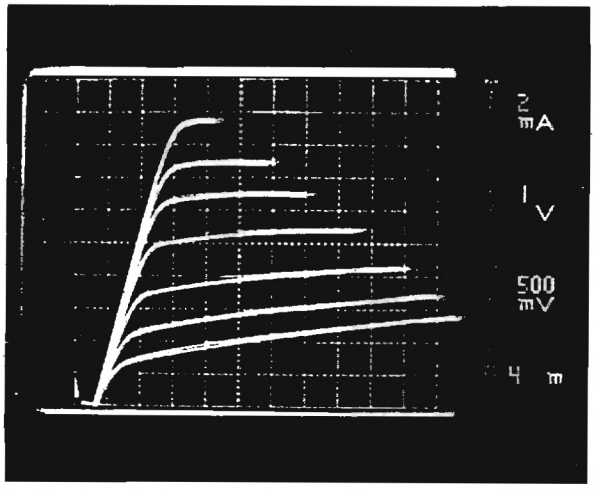
Schottky diode characteristics were measured on FETs fabricated during phase I. Gate metallization for these FETs was deposited by RF sputtering and consisted of Ti-Pt-Au. Devices available for test were from FETs which required second level metal to interconnect the source. Since second level metal was not developed in phase I, only portions of the devices were accessible.

The mixer diode equipment and screen room area were used to make measurements on FETs from A3032-4-12 (MBE) and A3032-5-17B (VPE). Effective gate width was 90 microns as measured microscopically.

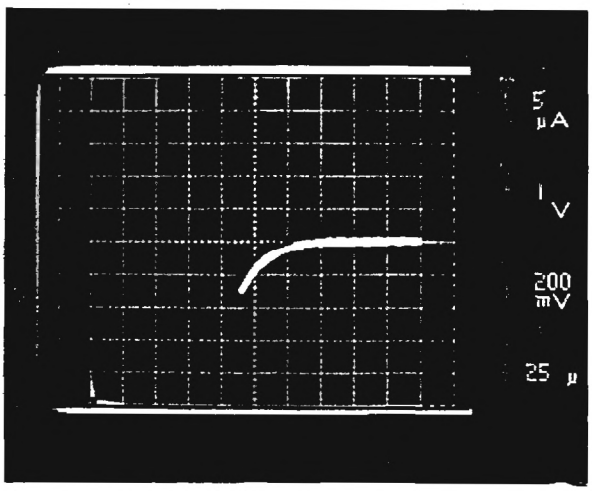
Figures 1 and 2 show transconductance, reverse breakdown, forward I-V and point by point data on a diode from A3032-5-17B and A3032-4-12 respectively. Ideality factors of 1.34 and 1.76 were calculated using the best fit mixer program. Saturation current was 2.68×10^{-11} A and 3.73×10^{-10} A respectively. These values are high when compared to mixer diodes fabricated at this lab. However, mixer diodes were fabricated on different material and Schottky metal depositon was by E-beam rather than sputtering. Additional data appears to be needed to accurately assess the quality of the sputtered schottky gates.

PLANS FOR NEXT MONTH

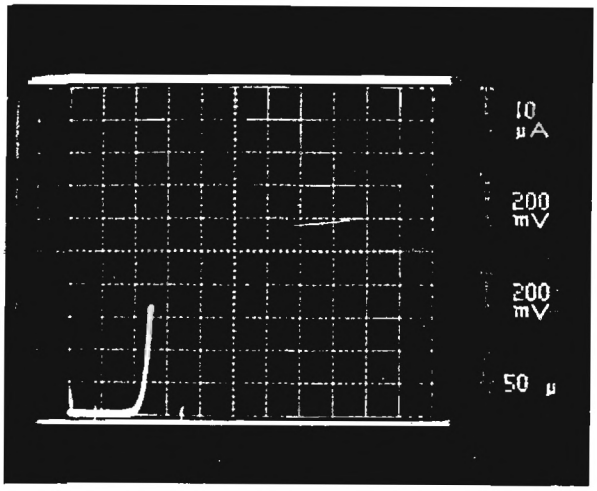
- Continue mask design effort
- Complete E-beam modification
- Further assess Schottky gate diode characteristics
- Begin air bridge process development



a. Transconductance



b. Reverse Breakdown



c. Forward I-V

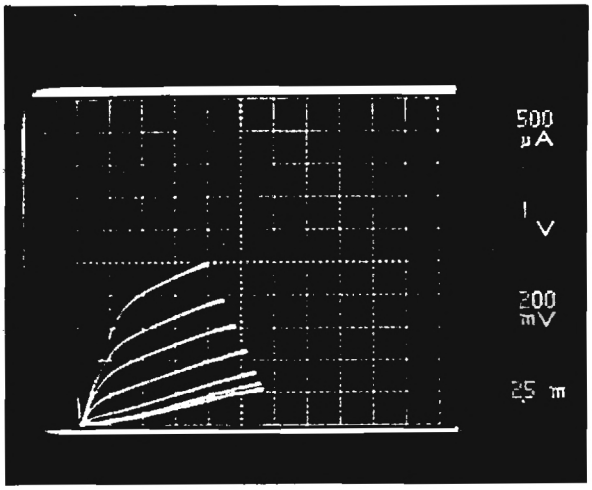
DIODE NUMBER 1.

IDEALITY FACTOR 1.34
RESISTANCE 30.11
SAT CURRENT 2.68-11

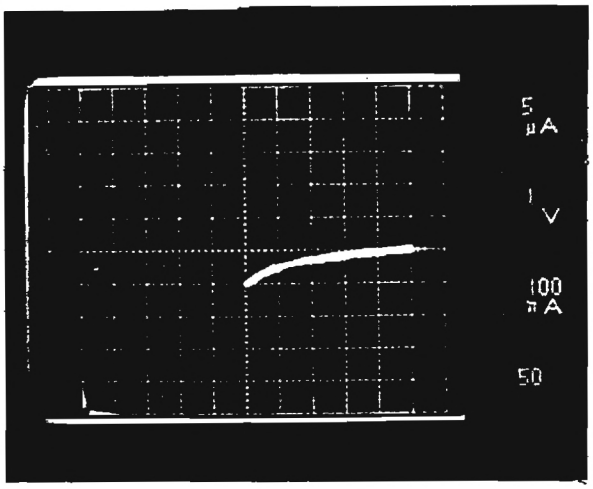
CURRENT UA	VOLTAGE VOLTS
0.010	0.165
0.100	0.277
1.000	0.377
10.000	0.447
100.000	0.520
1,000.000	0.630
3,160.000	0.755
10,000.000	0.999

d. Point by Point Data

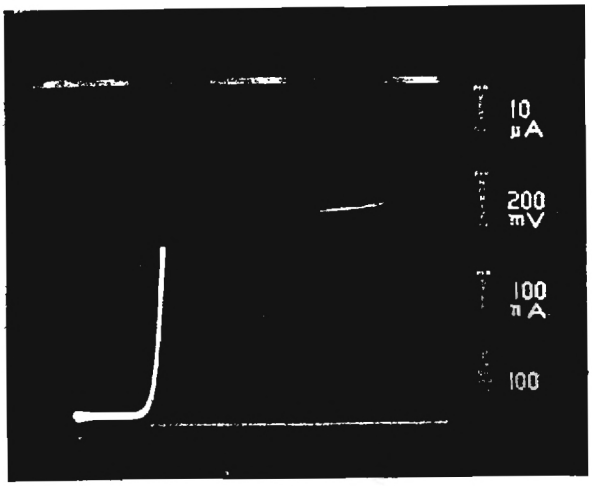
Figure 1. A3032-5-17B Data.



a. Transconductance



b. Reverse Breakdown



c. Forward I-V

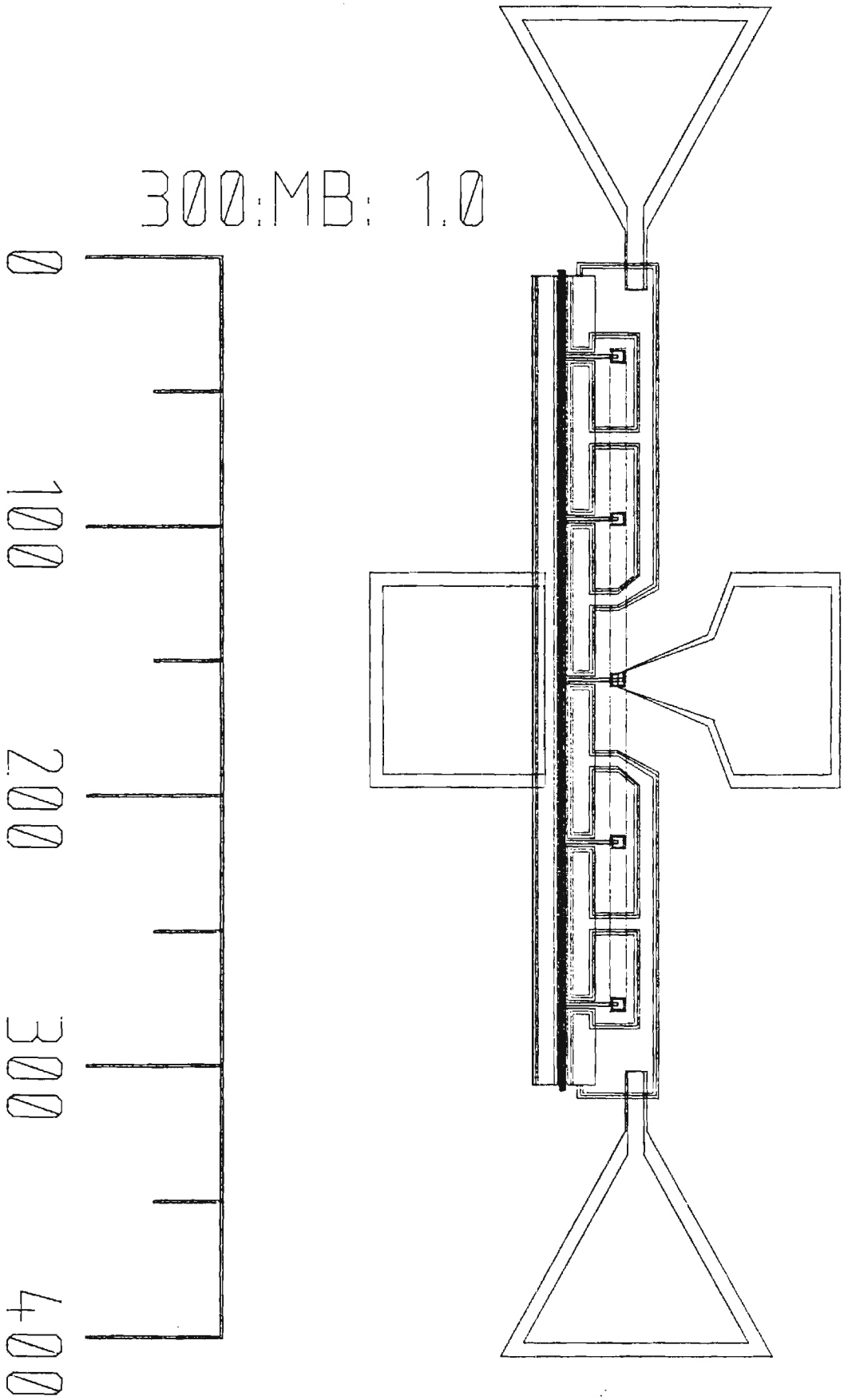
DIODE NUMBER 2.

IDEALITY FACTOR 1.76
RESISTANCE 20.60
SAT CURRENT 3.73-10

CURRENT UA	VOLTAGE VOLTS
0.010	0.050
0.100	0.233
1.000	0.391
10.000	0.469
100.000	0.557
1,000.000	0.731
3,160.000	0.979
10,000.000	0.999

d. Point by Point Data.

Figure 2. A3032-4-12 Data.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100
200
300
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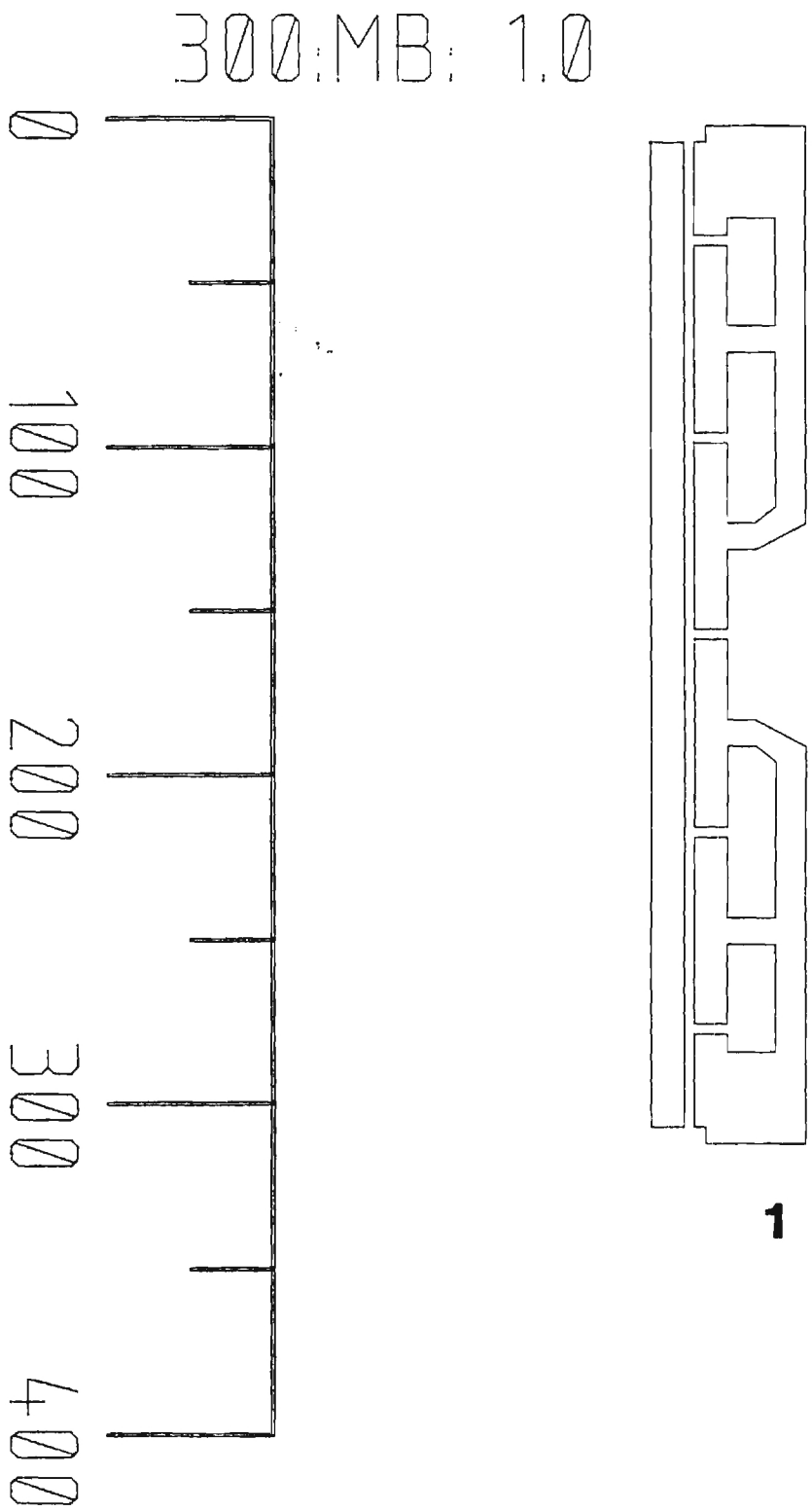

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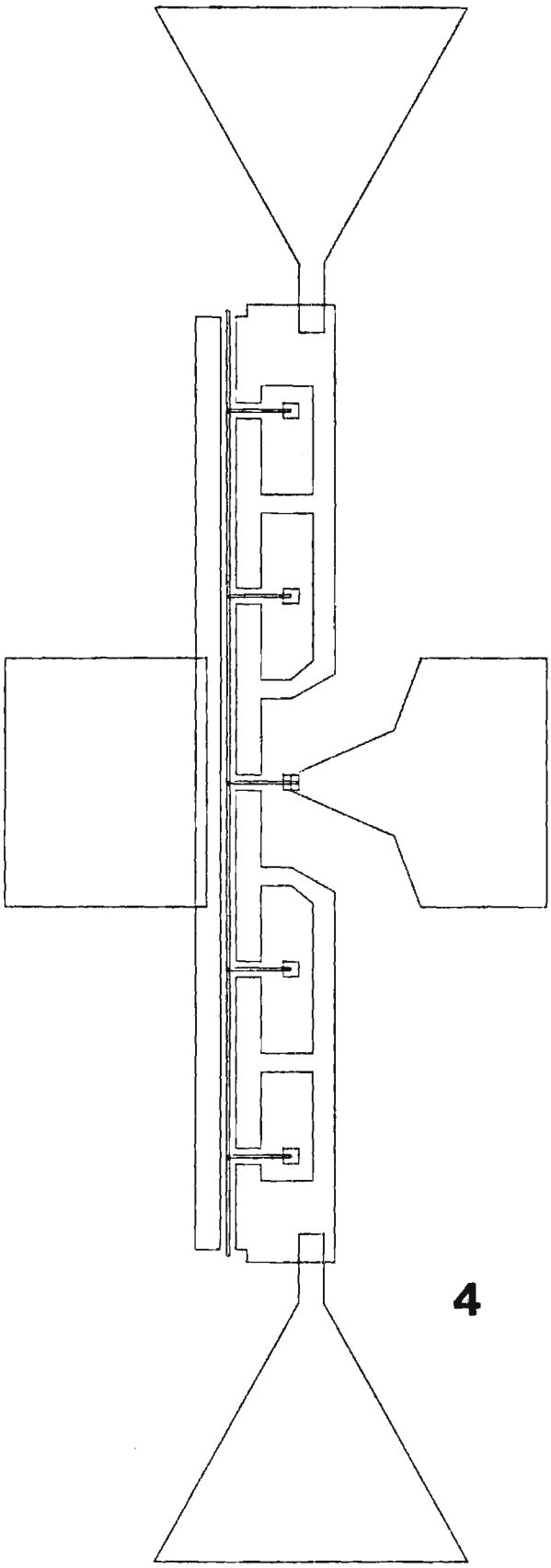

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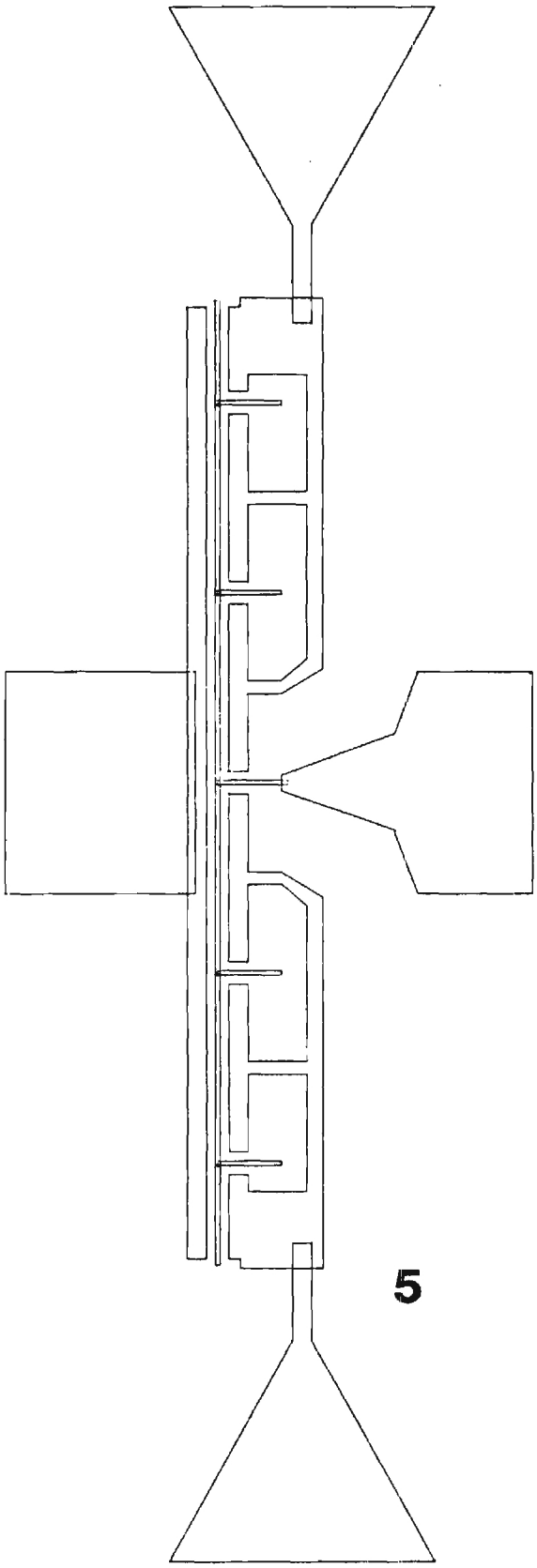

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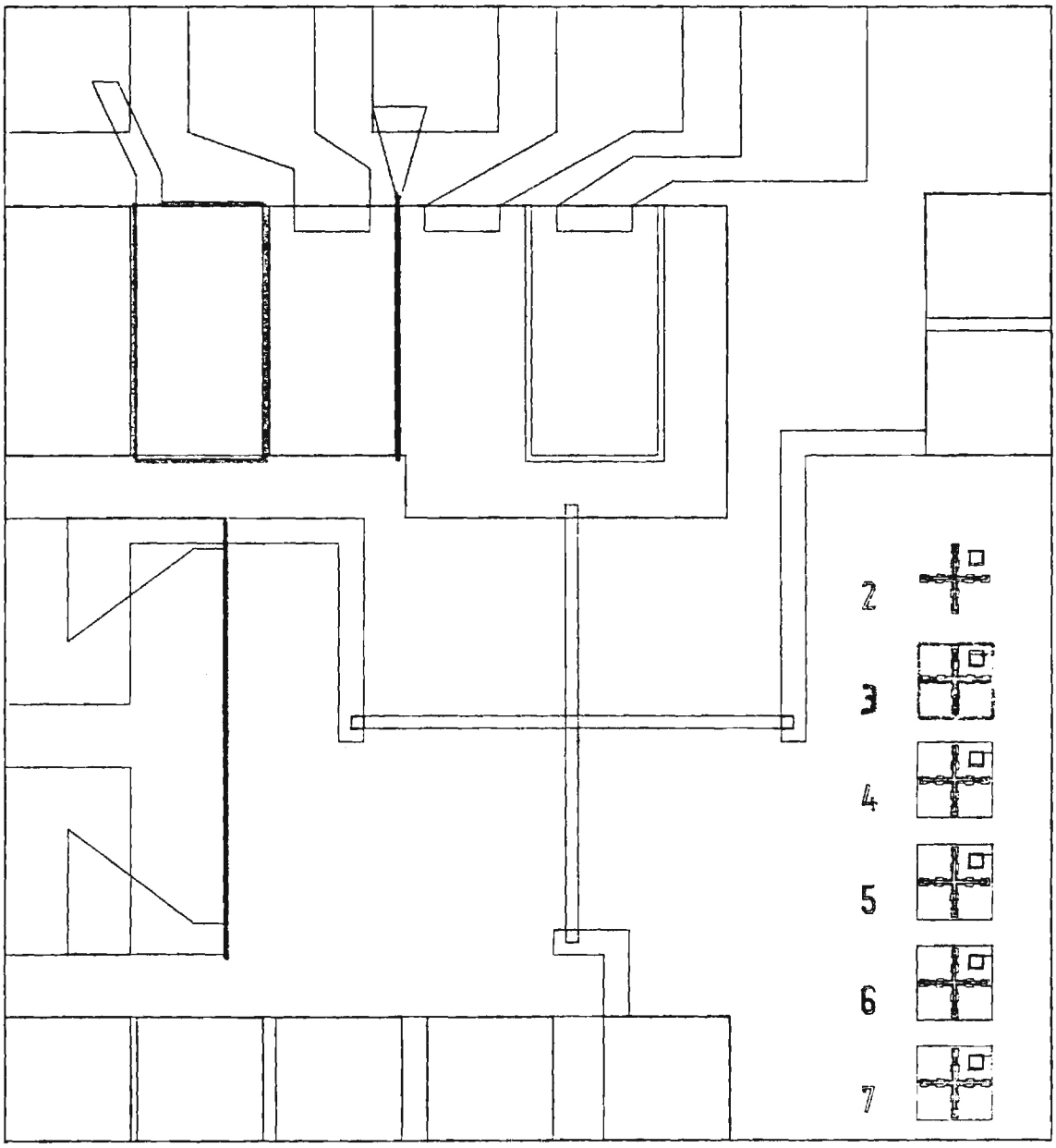
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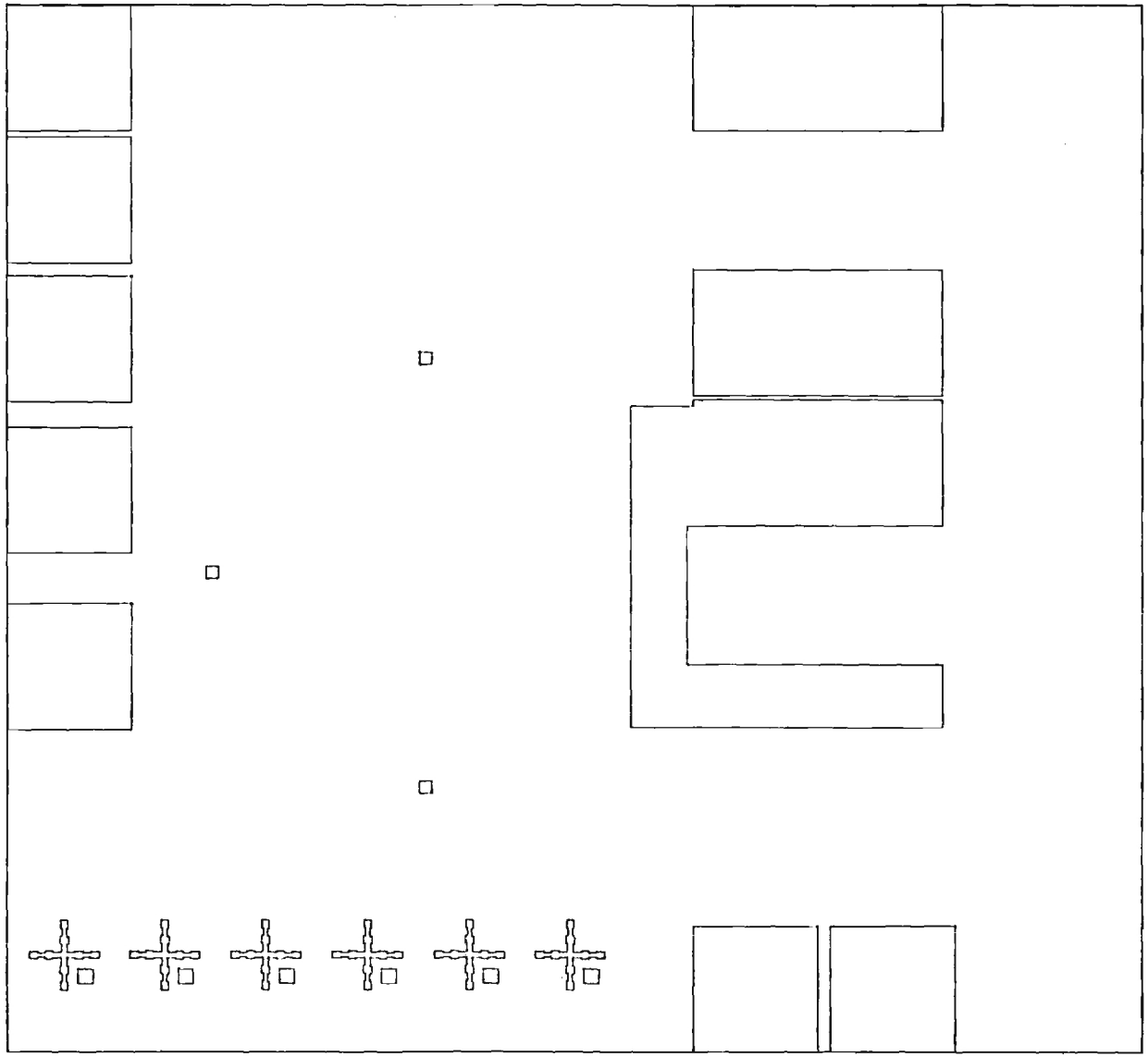

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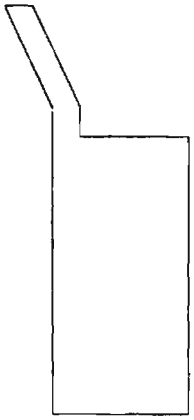

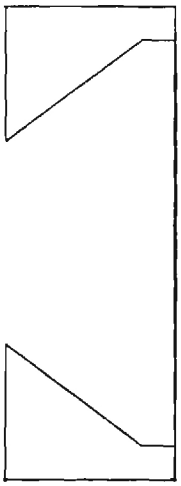

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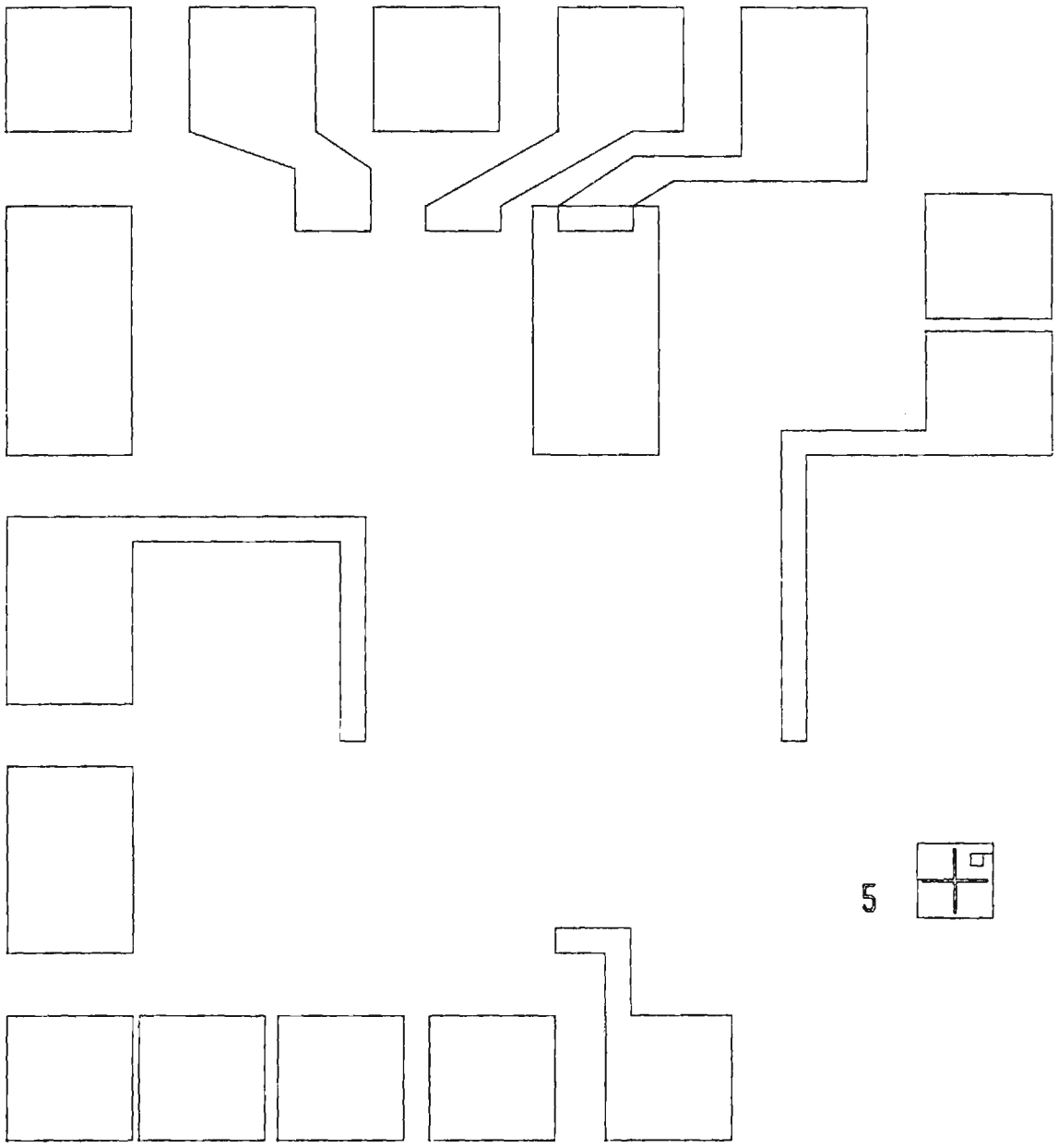
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A-3459

Del No. 5

Status Report 3

LOW NOISE GaAs FET - PHASE II

Contract period covered
1 March 1983 through 31 March 1983
P.O. No. S8-879406-LPY

A-3459

Submitted to
Hughes Aircraft Company
El Segundo, California 90245

by
Physical Sciences Division
Electromagnetics Laboratory
Engineering Experiment Station
Georgia Institute of Technology
Atlanta, Georgia 30332

Contracting through
Georgia Tech Research Institute
Georgia Institute of Technology
Atlanta, Georgia 30332

April 14, 1983

INTRODUCTION

This report describes the work performed on the program during the month of March. Planned modifications to the electron beam deposition system have been completed. Changes to the mask set design are being implemented. Process details are being formulated.

TECHNICAL EFFORT

Contract Item 2 - Define Mask Set

As discussed last month, several changes in the preliminary mask design were proposed to improve performance and ease of evaluation. In addition to the proposed changes, a review of technical report, "Low Noise K Band GaAs FET and Amplifier," (1) provided by the sponsor, disclosed information on additional changes that should improve the ease of fabrication and device performance. As as a result of this ERADCOM report prepared by Avantek and the previously noted design changes, a radical mask set redesign was initiated.

The Avantek process, used to fabricate 75 micron wide, subhalf-micron "M121" GaAs FETs, involves the following masking steps: (1), (2), (3), (4)

LEVEL #	DESCRIPTION
1	Mesa
2	Ohmic
3	Wide Gate Recess
4	Narrow Gate and Pads
5	Gate Plate
6	Vias for Air Bridge
7	Air Bridge

With exception of the order of the first and second mask levels, the Avantek procedure is the same as the one proposed for this effort. An advantage of etching the mesa prior to ohmic deposition (Avantek process) is the fact that more complete coverage of the mesa is possible. Also ohmic metal can be extended to the contact pad region with no deleterious effects.

Deposition of ohmic contacts prior to mesa etch (RFIC process) allows for a more accurate determination of mesa isolation by electrical probing. In a production environment where all the epitaxial active layers are grown in-house, this measurement is much less important than it is in an R and D program. As a result of the need to electrically measure mesa isolation, the order of masking was not changed.

Gate to source spacing of the M121 FET is 1.0 microns while the drain to source spacing is 3.5 microns. These dimensions appear to be conservative considering that Avantek is producing sub half-micron gates. However, it is probable that Avantek has learned that these dimensions provide acceptable device yield with respect to photolithography. Based on these considerations, 1.0 and 3.5 micron distances were selected for gate to source and drain to source dimensions. Additional design rules are shown in table 1 for unbridged devices and table 2 for bridged structures.

Attached is a plot of the new design for air bridge devices. This plot does not contain all levels, but does show the basic overall design of a 0.25 micron gate length device 75 microns wide. Design changes are scheduled to be complete by the end of April to allow for formal review.

UNBRIDGED DEVICES

APPLICATION	DIMENSIONS (microns)	LEVEL TO LEVEL
gate widths	75, 150, 300	mesa to mesa
mesa length	23.5	mesa to mesa
mesa segment separation	10.0	mesa to mesa
drain to source spacing	3.5	ohmic to ohmic
gate to source spacing	1.0	ohmic to narrow gate
gate runoff of mesa	2.0	narrow gate to mesa
gate feed lines	4.0	narrow gate to narrow gate
narrow gate metal withdrawn 2.0 microns from ohmic edges nearest gate region	2.0	narrow gate to ohmic
narrow gate metal withdrawn 1.0 microns from ohmic metal elsewhere	1.0	narrow gate to ohmic
plated gate metal coincident with narrow gate metal on ohmics,	0	plated gate to narrow gate
one (1) micron wider on each side of gate feed,	1	plated gated to narrow gate
withdraw one micron on pads	1	plated gate to narrow gate
via opening withdrawn 2.0 microns from edge of plated gate level on pads	2	via to plated gate
air bridge metal coincident with plated gate level	0	air bridge to plated gate
bond pad area > 2 x 2 of free bonding area	2x2 mils	

Specific Dimensions

Gate Length (microns)	Wide Gate (microns)	Plated Gate (microns)
.25	.75	1.0
.50	1.0	1.5
.75	1.25	2.0
1.0	1.5	2.0

Table 1. Unbridged Device Dimensions.

BRIDGED DEVICES

APPLICATION	DIMENSIONS (Microns)	LEVEL TO LEVEL
gate widths	75, 150, 300	-
mesa length	15.5	mesa to mesa
drain to source spacing	3.5	ohmic to ohmic
gate to source spacing	1.0	ohmic to narrow gate
gate runoff of mesa	2.0	narrow gate to mesa
narrow gate metal withdrawn 2.0 microns from ohmic edges nearest gate region	2.0	narrow gate to ohmic
narrow gate metal withdrawn 1 micron elsewhere	1.0	narrow gate to ohmic
plated gate metal coincident with narrow gate metal on ohmic	0	plated gate to narrow gate
plated gate metal withdrawn 1 micron on pads	1.0	plated gate to narrow gate
via opening withdrawn 2.0 microns from edge of plated gate level	2.0	via to plated gate
air bridge plate coincident with plated gate level on pads	0	air bridge to plated gate
bond pad area > 2 x 2 mils of free bonding area	2 x 2 mils	-

Specific Dimensions
(microns)

Gate Width	Gate Length	Mesa Split Width	Gate Feed Width	Wide Gate Length	Plate Gate Length	Air Bridge Length	Via	Source Interconnect
75	.25	6	3	.75	1.0	10	6 dia.	8
	.50	6	3	1.00	1.5	10	6	8
	.75	6	3	1.25	2.0	10	6	8
	1.00	6	3	1.50	2.0	10	6	8
150	.25	10	5	.75	1.0	15	6x11	10
	.50	10	5	1.00	1.5	15	6x11	10
	.75	10	5	1.25	2.0	15	6x11	10
	1.00	10	5	1.50	2.0	15	6x11	10
300	.25	10	5	0.75	1.0	20	6x16	12
	.50	10	5	1.00	1.5	20	6x16	12
	.75	10	5	1.25	2.0	20	6x16	12
	1.00	10	5	1.50	2.0	20	6x16	12

Table 2. Bridge Device Dimensions.

Contract Item 3 - Modify E-beam System

Planned modifications to the electron beam evaporation system have been completed. Modification of the substrate holder and emission opening now permit deposition of Ti, Pt and Au while maintaining the substrate temperature below 125°C. However, deposition rates were lower than expected. The small amount of source material was considered a possible cause of the low deposition rate since the new substrate position is not directly above the hearth but located at an angle of approximately 45°. Due to the depth of the source material compartments, shielding from the top of the hearth is possible when a small amount of source material is present.

Disassembly of the main vacuum chamber was performed, and the new four crucible hearth was installed. Carbon crucibles were machined for the Pt and Au positions, and new source materials of Ti, Pt, Au and W were loaded. Tungsten was included as a possible replacement for Pt which is very difficult to pattern with techniques other than lift-off.

After loading the sources, deposition yield was improved for Ti, Pt and Au. However, W could not be evaporated even at 3.8 kW (the maximum available power for this E-gun). Although W could not be evaporated, the system can be used for Ti, Pt, and Au and can easily be converted back to the original configuration for mixer diode fabrication. A Ti/W sputtering target has been ordered to evaluate its use as a suitable gate material. Sputtering is the method employed by Avantek for gate metal deposition.

Contract Item 4 - Procure GaAs Epitaxial Material

Three 2" diameter wafers have been ordered from Raytheon. Receipt of the first wafer is expected by the end of April. Other wafers will be delivered as needed after evaluation of previous wafers.

Contract Item 5 - Develop Air Bridge and Second Level Metal Process

Low gate resistance is critical in obtaining good low noise characteristics at high frequency. Multiple gate feeds reduce the gate resistance at the expense of a more complex fabrication process. Bridging of the gate metal over the source is the approach proposed in this work, and is the design used by Avantek. Bridges, 10 microns long, are being designed for 75 micron wide devices. Bridges, 15 and 20 microns, will be employed on 150 and 300 micron devices respectively. Minimum via contacts will be 6 microns in diameter and larger where applicable. Two bridges are required for 75 and 150 micron devices having 3 gate feeds. Four bridges will be utilized on the 300 micron devices.

Fabrication steps involved in this process involve:

Vias - to contact plated gate metal

Metal deposition - to provide a contact layer for plating

Air bridge Photoresist - to open areas for the air bridge metal

Electroplate - to provide a thick metal layer which constitutes the bridge

Photoresist Removal

Thin Metal Etch - to isolate the desired air bridge metal

Photoresist Removal -

Air bridge processes have been developed at this lab for use with

IMPATT diodes (5). This experience will be used to tailor a process to meet the requirements of this application. Photoresist thicknesses and profiles are of primary concern. Plated metal thickness is important from a mechanical and electrical standpoint. Air bridge metal thickness similar to Avantek's is expected. Process development experiments using the RFIC mask set are planned for next month.

PLANS FOR NEXT MONTH

- Continue mask design effort
- Conduct a formal review of the mask design
- Continue air bridge development

REFERENCES

1. C. Huang, etal. "Low Noise K-Band GaAs FET and Amplifier," Interim Technical Report, ERADCOM, Fort Monmouth, N.J. July 1980.

2. W. Kennan, etal. "Low Noie K-Band GaAs FET and Amplifier," Final Report, ERADCOM, Fort Monmouth, N.J. January 1983.

3. C. Huang, etal. "Microwave Gallium Arsenide FET Amplifiers," Annual Report, NRL, Washington, D.C. April 1982.

4. R. Thill, etal. "A Low Noise GaAs FET Preamplifier for 21 GHz Satellite Earth Terminals." Microwave Journal, March 1983.

5. C. Rucker, "Millimeter Wave Chip Combining," Final Technical Report, AFWAL, To be published.

Del No. 7

Status Report 4

LOW NOISE GaAs FET - PHASE II

Contract period covered
1 April 1983 through 30 April 1983
P.O. No. S8-879406-LPY

A-3459

Submitted to
Hughes Aircraft Company
El Segundo, California 90245

by
Physical Sciences Division
Electromagnetics Laboratory
Engineering Experiment Station
Georgia Institute of Technology
Atlanta, Georgia 30332

Contracting through
Georgia Tech Research Institute
Georgia Institute of Technology
Atlanta, Georgia 30332

May 10, 1983

INTRODUCTION

This report describes the work performed on the program during the month of April. A program review was held on April 27 and emphasized mask layout. Micro Mask Inc. was contacted, and preliminary plots of the mask set were sent for their review. Air bridge evaluation masks were designed and fabricated at Ga. Tech. The electron beam power supply problem has been identified.

TECHNICAL EFFORT

Contract Item 2 - Define Mask Set

Proposed mask design changes were made and plots were prepared for the program review. During the program review, it was mentioned that critical dimensions should be located on quarter micron grids to facilitate E-beam mask generation. A phone call to Micro Mask Inc. (Bob Parille of the Fla. office) confirmed the need for this layout, and he also made other helpful suggestions. Bob sent a data package which included mask fabrication travelers as well as specific design rules recommended by the mask manufacturer. He graciously offered to evaluate our initial design, so plots were promptly sent to him. Progress on this task is on schedule and tapes of the layout should be completed by mid-May. These tapes will be either GDS II or Mebes format.

Contract Item 3 - Modify E-beam System

As discussed during the program review, full power could not be obtained with the electron beam deposition system when attempting to evaporate tungsten. Partial disassembly of the

system has disclosed the necessity of changing three transformer tapes to obtain full power (6 Kw) on the 20 kV range. These changes will be made and another attempt made to evaporate tungsten. These efforts are considered to be worthwhile due to the cleanliness of the E-beam vacuum system and the potential for surface damage should RF sputtering be reqired for gate metal deposition.

Contract Item 4 - Procure GaAs Epitaxial Material

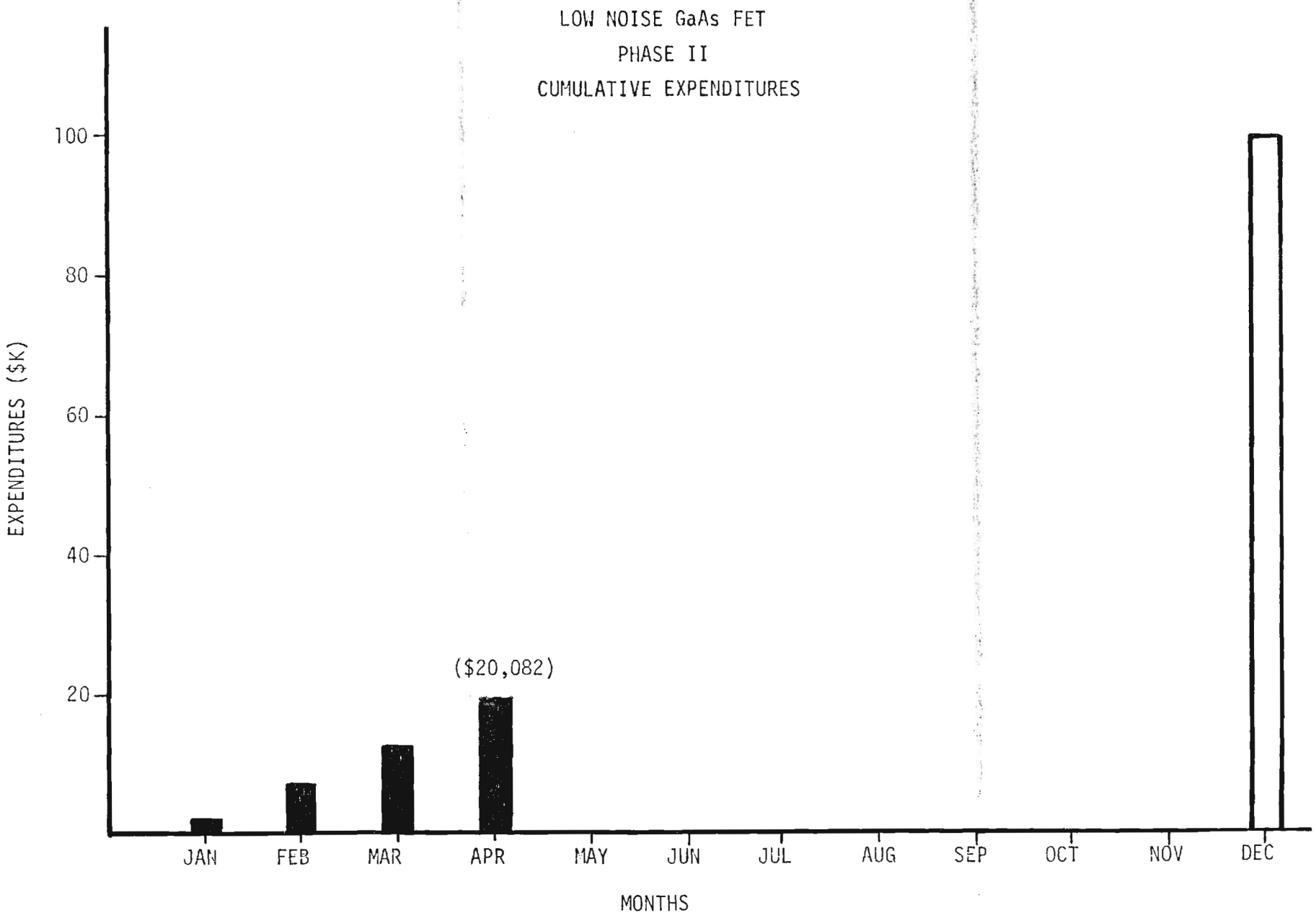
The first of three wafers is scheduled for shipment during the vendor's April monthly shipments.

Contract Item 5 - Develop Air Bridge and Second Level Metal Process

Air bridge evaluation structures have been designed using the Calma system. Rubylith was successfully scribed on the HP plotter using a cutter designed and built at Ga. Tech. Excellent patterns were obtained after peeling the unwanted rubylith. Photomasks were made using a fly's eye camera system. Minimum line widths on these patterns were 2 microns. Inspection of the masks after development indicated that the minimum geometries were not well defined. Photoresist tests on bare silicon wafers are in progress to determine whether or not these masks are usable for the air bridge process evaluation.

PLANS FOR NEXT MONTH

- o Check mask design and generate tapes
- o Repair E-beam power supply and attempt to evaporate tungsten
- o Continue air bridge process development using Ga. Tech generated mask or RFIC mask set
- o Prepare Ti-W sputtering target as a back up for gate metal deposition.


LOW NOISE GaAs FET
PHASE II
CUMULATIVE EXPENDITURES
EXPENDITURES ($K)
100
80
60
40
20
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JAN
FEB
MAR
APR
MAY
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JUL
AUG
SEP
OCT
NOV
DEC
MONTHS

Del No. 10

Status Report 5

LOW NOISE GaAs FET - PHASE II

Contract period covered
1 May 1983 through 31 May 1983
P.O. S8-879406-LPY

A-3459

Submitted to
Hughes Aircraft Company
El Segundo, California 90245

by

Physical Sciences Division
Electromagnetics Laboratory
Engineering Experiment Station
Georgia Institute of Technology
Atlanta, Georgia 30332

Contracting through
Georgia Tech Research Institute
Georgia Institute of Technology
Atlanta, Georgia 30332

June 6, 1983

INTRODUCTION

This report describes the worked performed on the program during the month of May. Micro Mask Inc. has provided inputs on the mask layout. Another domestic mask maker (Sienacin) has been contacted and has expressed an interest in producing the photomasks. Air bridge evaluation masks were improved and processing initiated. GaAs epitaxial material was received. The electron beam power supply problem has been corrected and tungsten evaporation attempts have been made. A Ti/W sputter deposition target has been received and mounted.

TECHICAL EFFORT

Contract Item 2 - Define Mask Set

Mask design plots have been evaluated by Micro Mask (Sunnyvale). Currently their minimum beam diameter is .25 micron and as a result they are reluctant to try to pattern the .25 micron lines which we desire. However, they said they would attempt the .25 micron features with no guarantee on the results. Micro Mask personnel indicated that they could delineate .5 micron features provided that these features are clear on the mask rather than chrome. Since the gate lines are clear on the mask we should be able to obtain working plates having .5, .75 and 1.0 micron gates. It is also possible that some of the .25 micron gates will be acceptable.

Discussions with CAD personnel at Micro Mask indicated that

they can accept a Calma data base tape of the type CDS II Rev. 3. Specified path types must be D, 1 or 2 only. text fonts must either be digitized or produced with tape which Micro Mask provides.

All critical device dimensions have been placed on .25 micron grid lines. Text editing using the Micro Mask tape is the only remaining task to be completed before generating the data base type.

Sierracin/EOI, an E-Beam mask maker in Irvine, Ca., has been contected. Using a Varian E-Beam system, they are also working with a .25 micron spot size like Micro Mask, but indicated that if a particular pattern is not dense, through some chemical processing changes they could possibly achieve .25 micron clear lines. They have agreed to try to make an evaluation mask. A GDS II Rev. 4 tape having the narrow gate and plated gate levels is being prepared for their evaluation attempt.

Contract Item 3 - Modify E-Beam System

Full E-gun power has been obtained by changing three transformer taps. System disassembly was performed to realign the gun with respect to the sample crucible position to obtain optimum performance.

Several attempts were made to evaporate tungsten without success. At full power (6 KW) no sign of melting was observed. With the existing E-gun, it appears that tungsten evaporation is not possible. Ti-Pt-Au deposition by E-beam evaporation is

available as well as sputter deposition of Ti/W.

The Ti/W target has been received and mounted in the sputtering system. Experiments are in progress to determine deposition rate, Schottky barrier quality and pattern delineation techniques.

Contract Item 4 - Procure GaAs Epitaxial Material

Three wafers were received from Raytheon. Only one was requested at a time to allow for evaluation and possible changes in the epi specifications. Visually all wafers were acceptable, having no haze and minimal random defects. Wafer 15H10 was retained due to its smaller active layer thickness and its near flat doping profile at the high concentration. Doping tails were similar on all three wafers. Undoped substrates were used to fabricate these epi layers. Quality assurance data on wafer 15H10 is attached.

Contrast Item 5 - Develop Air Bridge and Second Level Metal Process

Photoresist tests on silicon wafers using the emulsion plates discussed in the previous monthly resulted in poor pattern delineation. Another set of emulsion plates was made using different exposure conditions. Geometries were much improved and chrome working plates were made from the emulsion masters. Figures 1-3 are 500X copies of the patterns used for this process development. Deposition, photoresist and plating experiments are

currently in progress with this mask set.

PLANS FOR NEXT MONTH

- Generate data base tape
- Provide tape to Sierracin
- Continue air bridge process development
- Evaluate Ti/W Schottky process
- Initiate thick gate metal process development

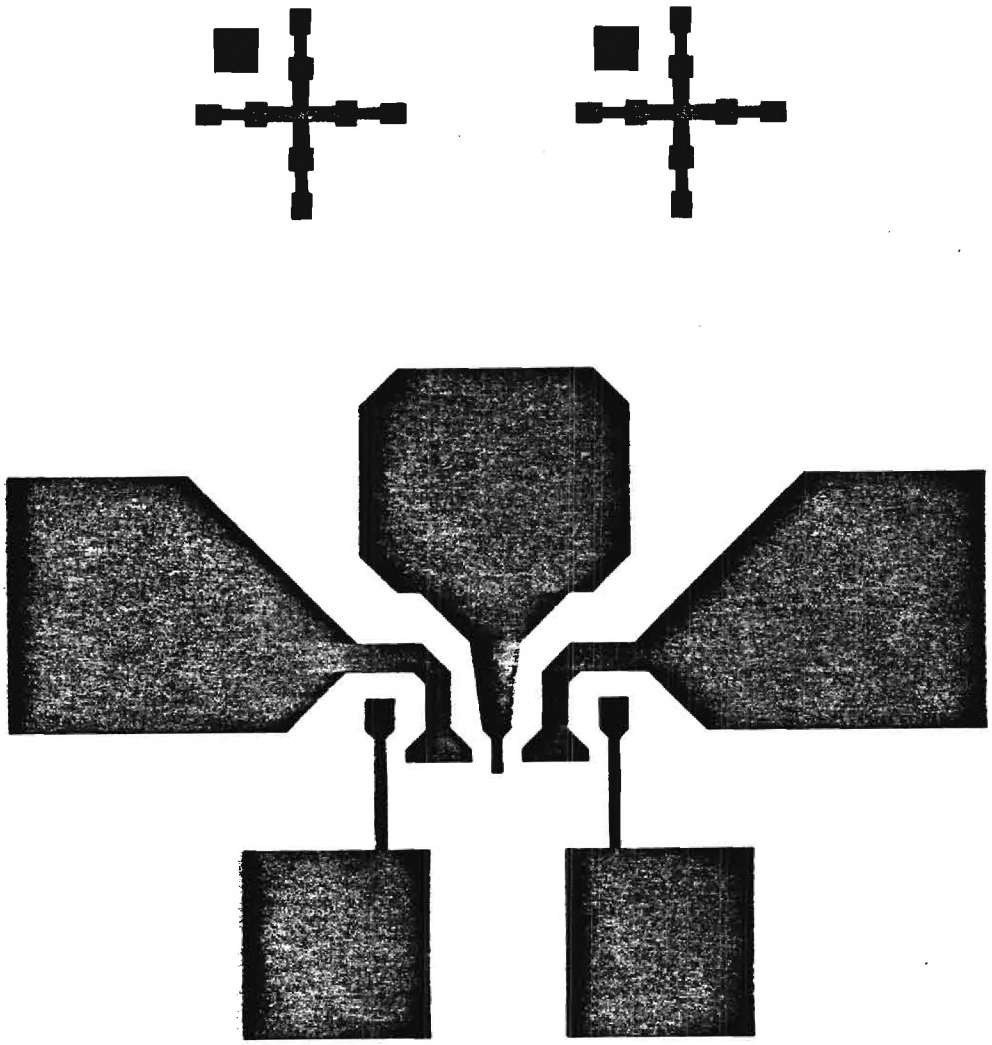


Figure 1. Reference Pattern.

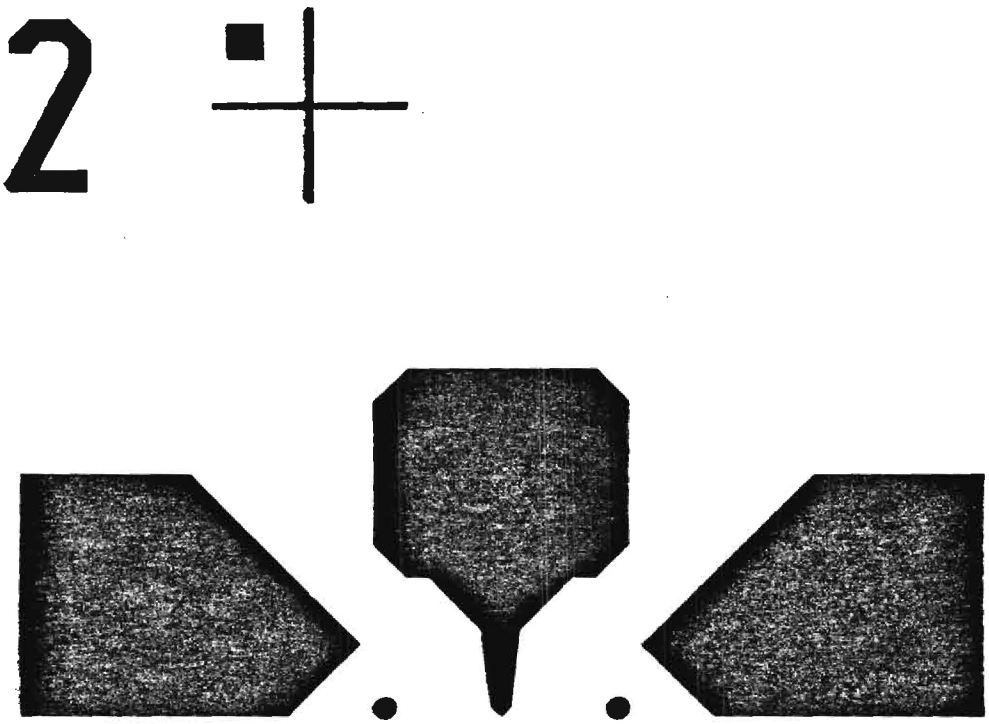


Figure 2. Via.

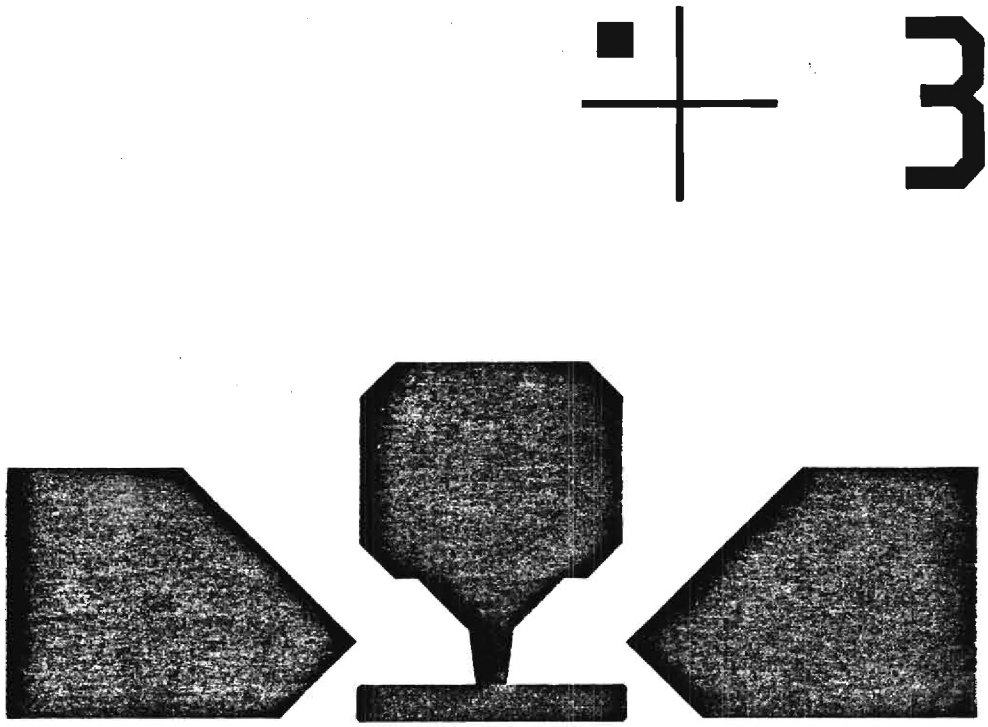
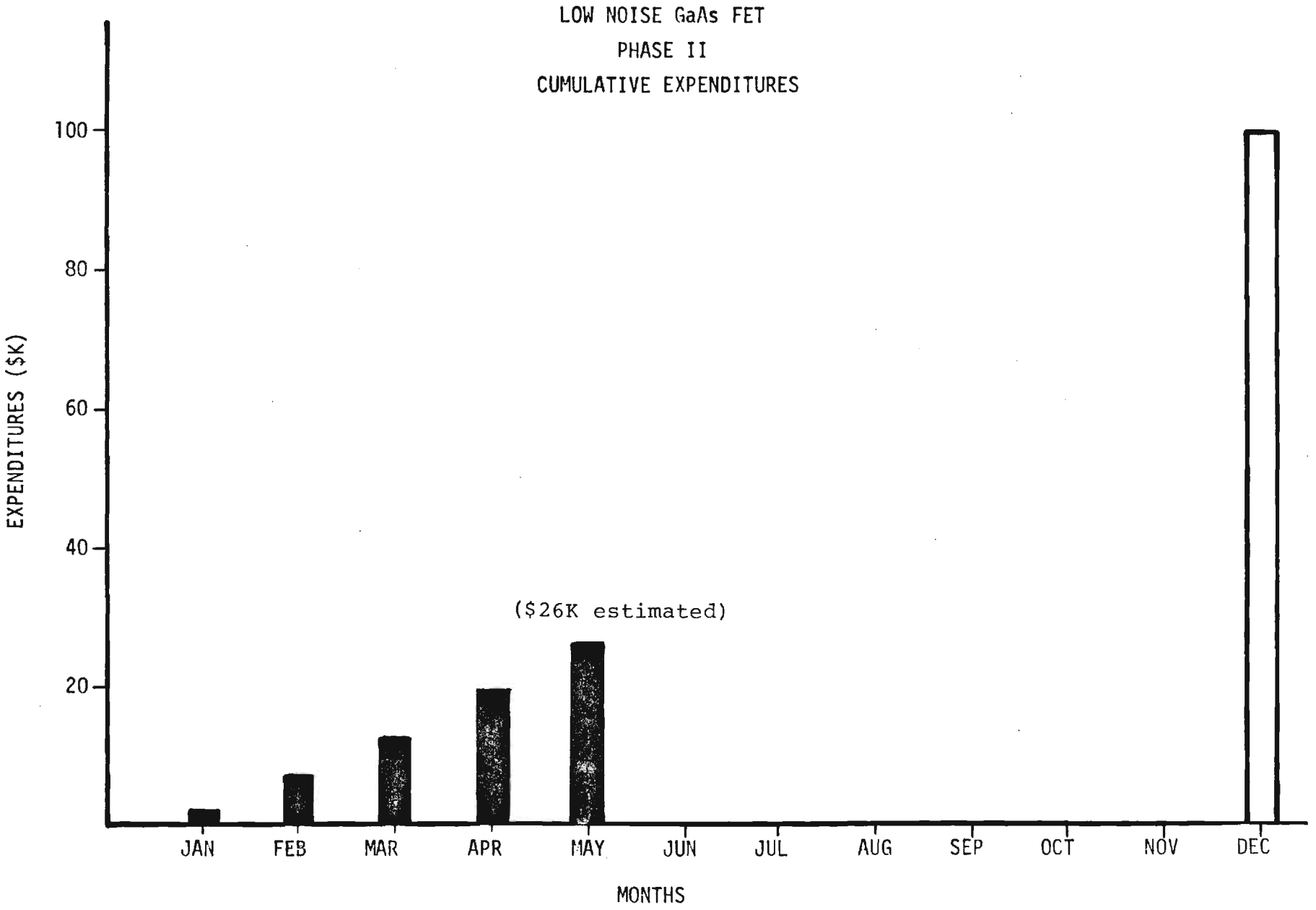


Figure 3. Air bridge.


LOW NOISE GaAs FET
PHASE II
CUMULATIVE EXPENDITURES
EXPENDITURES ($K)
100
80
60
40
20
($26K estimated)
JAN
FEB
MAR
APR
MAY
JUN
JUL
AUG
SEP
OCT
NOV
DEC
MONTHS

RAYTHEON

39-9083(3/83)

QUALITY ASSURANCE

GaAs Epitaxial Wafer NUMBER 15H10

For FET Type Devices |_| Low Noise |_| Power |_| Other _____

With |X| Buffer |_| Contact Layer

For IMPATT Type Devices |_| Flat Profile |_| Read Profile |_| Other _____

|_| Single Drift |_| Double Drift with |_| Thick Buffer |_| Standard Buffer |_| p** contact

Customer Georgia Inst. of Technology Customer Order No. GA3454-000-1-83-7144

Attention _____ Spec. No. _____

Sales Order No. 57448-10-7 Memo No. _____

RAMAC No. 31007

SUBSTRATE

Supplier Crystal Co Crystal Boule No. 167 Slice No. 31

Orientation 2° off 100 toward 110 Pregrowth Thickness 432 um

Carrier Concentration: NA 10^{18} cm^{-3} Dopant: Undoped

Resistivity** >10^7

ELECTRICAL CHARACTERISTICS

No.	Layer Type	Measured Carrier Concentration	Dopant	Thickness
1	Buffer	< x10^{14} cm^{-3}	NA	2.5 um
__	Buffer	x10 cm^{-3}		um
2	Active	16 x10^{16} cm^{-3}	Si	0.16 um
__	Active	x10^{16} cm^{-3}		um
__	Spike	x10^{17} cm^{-3}		( ) um
__	Contact	x10 cm^{-3}		(x_p) um

PHYSICAL CHARACTERISTICS

Wafer Size _____ cm Area 17.04 cm^2 Surface Morphology |_|

Q : _____ x $10^{12}e^{-}$-cm^{-2} V_{knee} _____ volts (from Cvs V curve)

C_o: _____ x 10^{4}pF-cm^{-2} Interface _____ um/decade

DELIVERY AUTHORIZATION

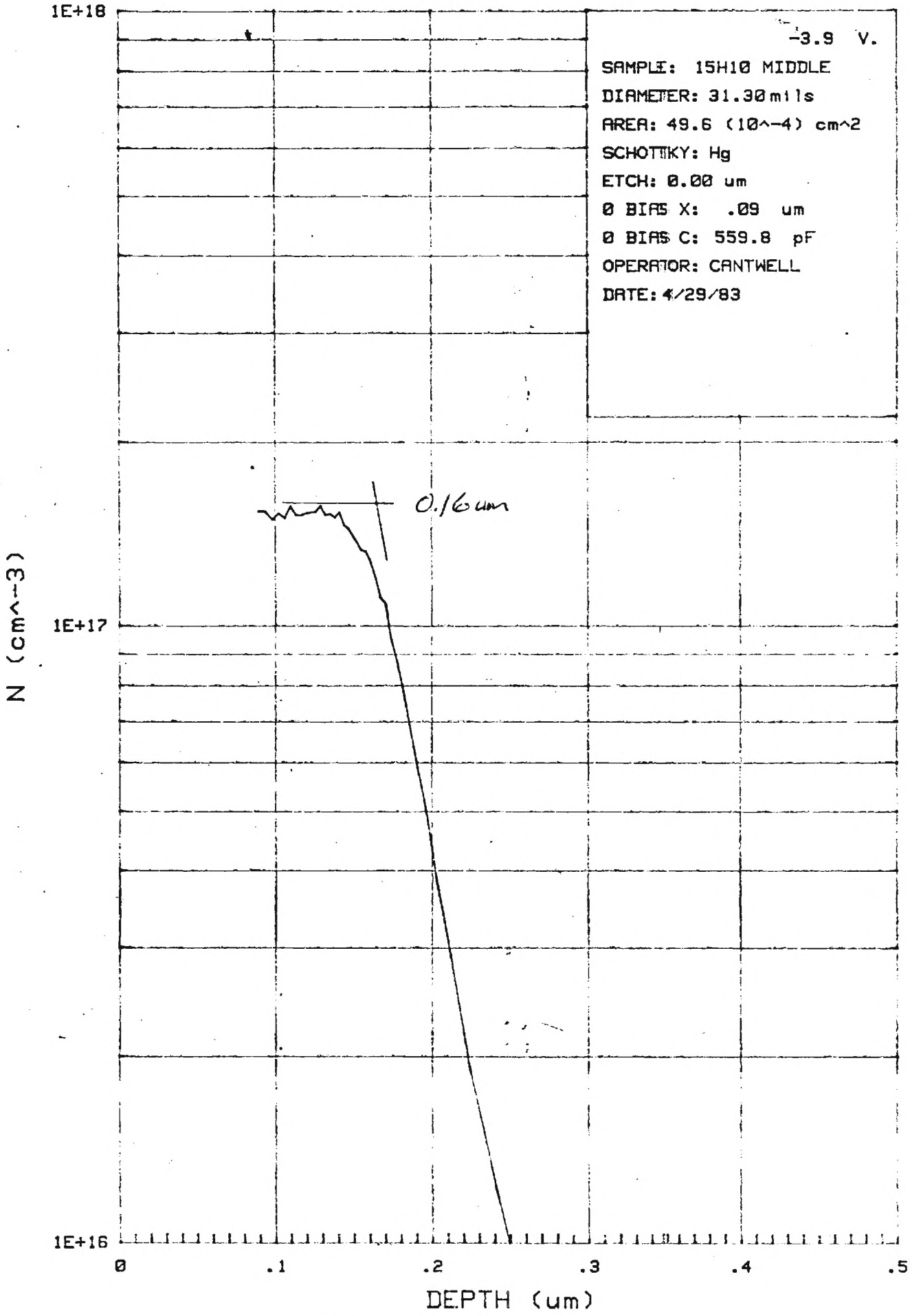
Delivery authorized |_| to fill order |_| to fulfill contractual obligations

|_| For Device Research |_| For Process Research |_| For Calibration

|_| For Sample Purposes Other _____

Amount Ordered 3 wafers Amount Delivered 3 wafers

BNeRe Date: _____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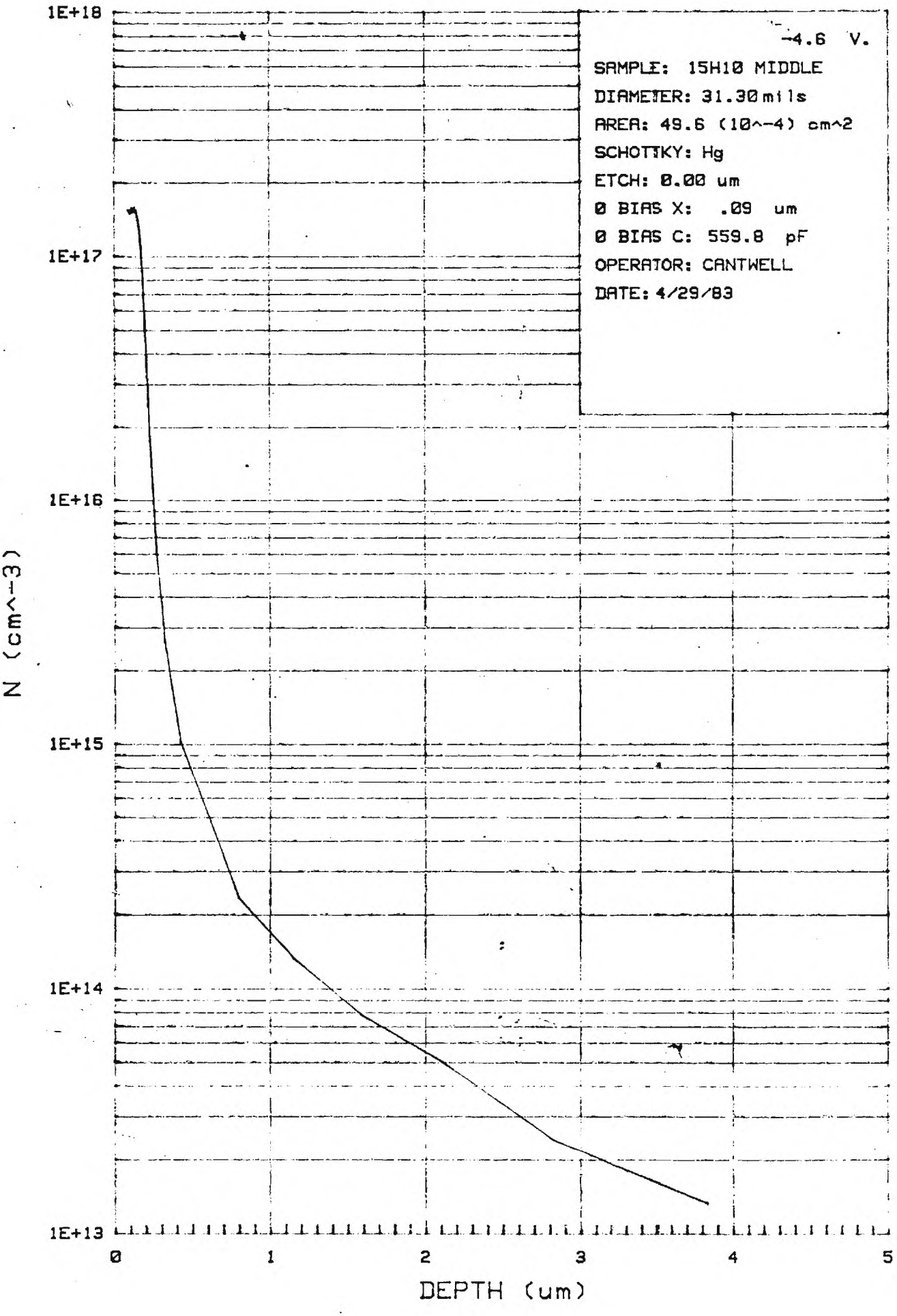
SAMPLE: 15H10 MIDDLE
DIAMETER: 31.30 mils
AREA: 49.6 (10^-4) cm^2
SCHOTTKY: Hg
ETCH: 0.00 um
0 BIAS X: .09 um
0 BIAS C: 559.8 pF
OPERATOR: CANTWELL
DATE: 4/29/83
0.16um
1E+18
1E+17
1E+16
N (cm^-3)
0
.1
.2
.3
.4
.5
DEPTH (um)


-4.6 V.
SAMPLE: 15H10 MIDDLE
DIAMETER: 31.30 mils
AREA: 49.6 (10^-4) cm^2
SCHOTTKY: Hg
ETCH: 0.00 um
0 BIAS X: .09 um
0 BIAS C: 559.8 pF
OPERATOR: CANTWELL
DATE: 4/29/83
1E+18
1E+17
1E+16
1E+15
1E+14
1E+13
N (cm^-3)
0
1
2
3
4
5
DEPTH (um)

Del. No. 13

Status Report 6

LOW NOISE GaAs FET - PHASE II

Contract period covered
1 June 1983 through 30 June 1983
P.O. S8-879406-LPY

A-3459

Submitted to
Hughes Aircraft Company
El Segundo, California 90234

by

Physical Sciences Division
Electromagnetics Laboratory
Engineering Experiment Station
Georgia Institute of Technology
Atlanta, Georgia 30332

Contracting through
Georgia Tech Research Institute
Georgia Institute of Technology
Atlanta, Georgia 30332

July 15, 1983

Introduction

This report describes the work performed on the program during the month of June. Final revisions to the mask layout were made and a tape sent to Micromask for processing. Another tape was sent to Sierracin/EOI to determine if Sierracin could define the .25 micron geometries. Air bridge evaluation masks were made and the air bridge process evaluated. The thick gate metal process is also being evaluated. Shallow UV optics have been installed on the Karl Suss aligner and optimization tests have begun.

Technical Effort

Contract Item 1 - Design Mask Set

After receipt of Micromask's text font tape, final modifications to the mask layout were made. A Rev. 3 stream tape was then produced containing the repeat pattern and all auxillary patterns. This tape, with a composite plot of the repeat pattern as well as composite and layer by layer plots of an individual device within the repeat pattern (.25 micron device), were sent to Micromask. An identical tape and more detailed plots (layer by layer of the repeat pattern included) were sent to Hughes.

A similar tape (Rev. 4) was generated and sent to Sierracin to evaluate their mask making capabilities. The narrow gate pattern as well as the plated gate pattern was included. Sierracin quickly informed us that lines not at 45° angles and any types of arcs were not compatible with their system. However, after discussion with Mr. Pete Avalos of Sierracin, the same tape was sent to Sierracin's facility in Santa Clara, California. An

evaluation was to be made to determine if they were capable of producing this mask set. No confirmation has been received to date.

Contract Item 4 - Develop Air Bridge process and Second Level Metal Processes.

Using the chrome plates developed for this process, we were able to fabricate the air bridges shown in Figures 1-4. These structures were created by first delineating a reference pattern on the wafer and sputtering gold onto the surface. After liftoff, the wafer was coated with photoresist (unthinned AZ-1350J, $\sim$ 1.5 - 1.7 microns thick). After delineating the via pattern in the photoresist, a thin layer of metal (Au) was sputter deposited. Photoresist was again applied and the bridge structure was delineated. Gold was then electroplated to build up the bridged device. The top layer of photoresist was removed and the wafer immersed into gold etch to remove the thin, sputtered layer. The remaining photoresist was then removed. Visual comparison of these bridges to the Avantek M121 device bridge was favorable

Contract Item 5 - Develop Thick Gate Metal Process

In order to develop a thick gate process, it was decided that a comparison should be made between the Schottky contact made with electron beam deposited Ti-Pt-Au and sputter deposited Ti/W-Au. In order to make this comparison, we relied on the work done by Jerry Hill on Mixer Diodes (Hughes contract P.O. No. S8-738203-LV3). In that previous work, mixer diodes fabricated with Ti-Pt-Au contacts were evaluated. Processing mixer diodes with the same mask but with a Ti/W contact has begun. This mask uses a photoresist on SiO_2 to achieve a metal break which facilitates liftoff. Figures 5-8 show the break in the photoresist - SiO_2 boundary. This

is quite an unusual profile. Although produced by mistake, it worked very well. The procedure outlined in Jerry Hill's work was followed up to the point of etching the photoresist with an O_2 plasma. At this point, the photoresist was over-etched and required another Hydrofloric etch to undercut the SiO_2. These photos show the resultant structure. Further tests would have to be made to determine if the process is repeatable. The metal would not lift off in acetone and required the tape method (i.e., mounting the wafer on a glass slide with wax, pressing mylar tape on it and pulling apart). This method was facilitated by soaking the wafer in ammonia before initiating the method. Evaluation of the devices has begun. In addition, dry plasma etching experiments on the Ti/W have been undertaken to determine the feasibility of etching the Schottky metal. To date, these experiments have not been successful.

Photoresist Considerations

It is well known that the shorter wavelength light you use to expose the photoresist, the smaller dimensions you can delineate. It is therefore with this consideration that we changed the optics on our aligner to UV optics - shallow UV in more precise terms. A test was run to determine how effective these optics were in delineating 1 micron linewidths. Exposure time increased to the range of 10 seconds (up from 3 sec.), while developing time remained the same at 45 seconds. Results are shown in Figure 9. The developed patterns showed good uniformity and edge acuity. However, the photoresist again begins to develop where two lines intersect before it begins to develop the lines. This might be taken into consideration in future mask designs. More optimization tests must be

performed. In addition, the superior qualities of this system will not be apparent until the new mask set arrives and we can test whether or not the shallow UV optics can define sub-micron geometries.

Plans for Next Month

° Continue thick gate process

° Evaluate Polyimide

° Measure Ti/W Schottky characteristics

° Follow up on mask fabrication

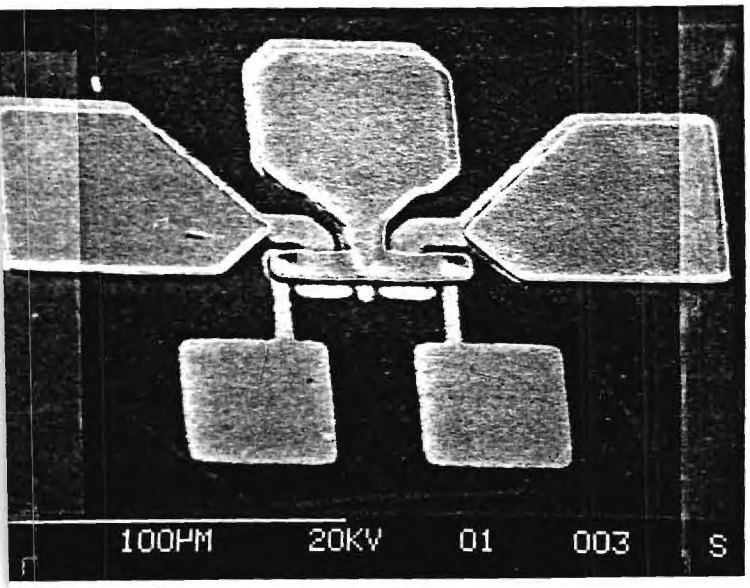


Figure 1. Overall Device Pattern

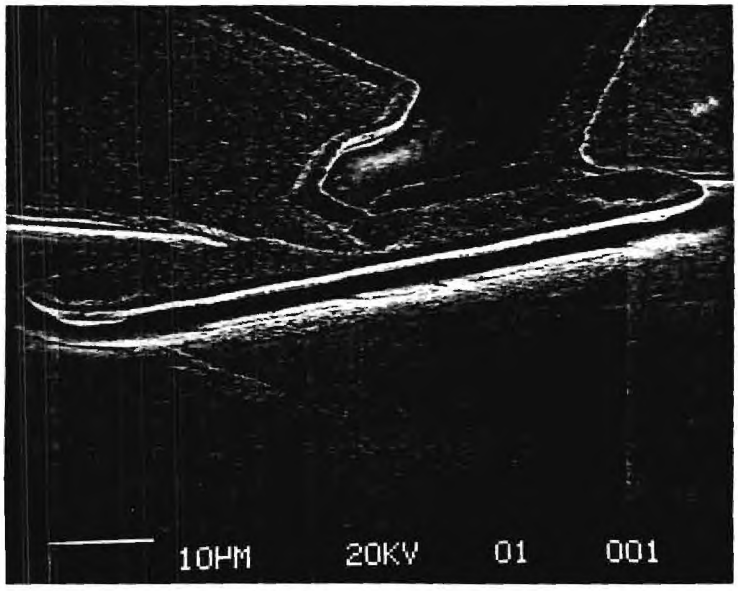


Figure 2. Plated Bridge Structure

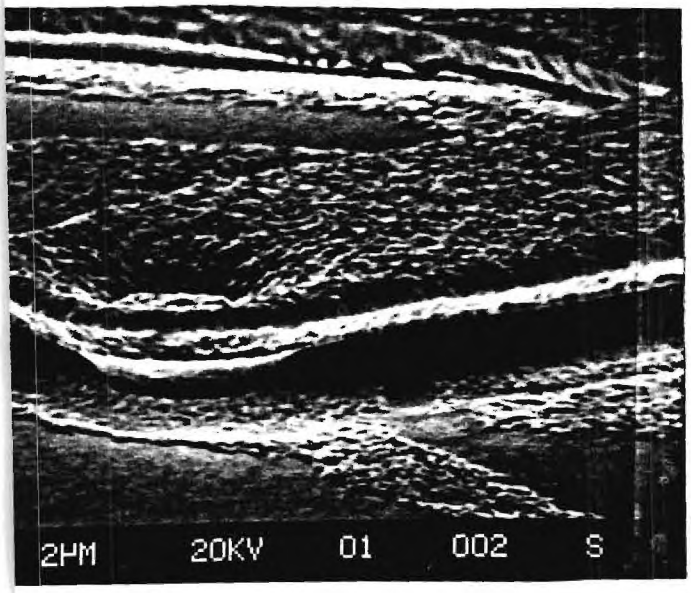


Figure 3. Via-centered

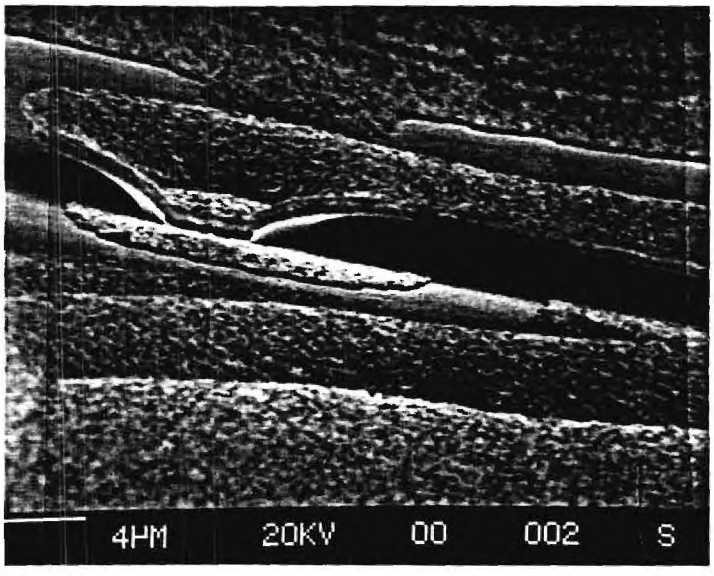


Figure 4. Via-off center

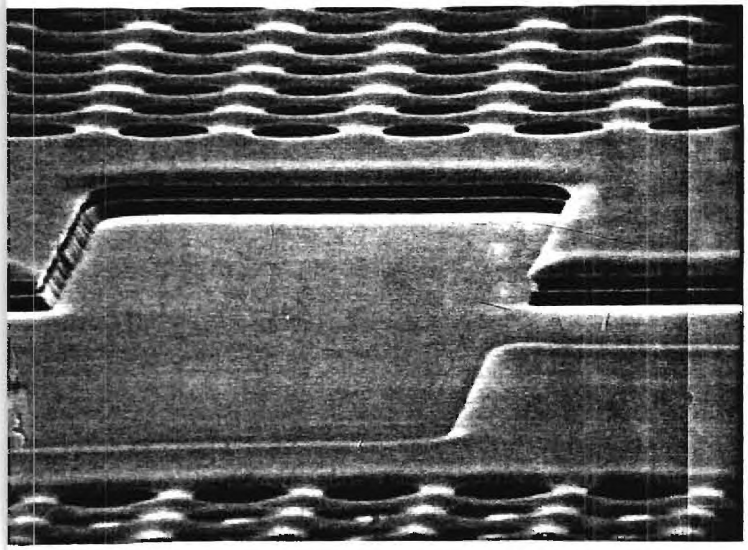


Figure 5. Large Pattern Showing SiO_2 photoresist structure.

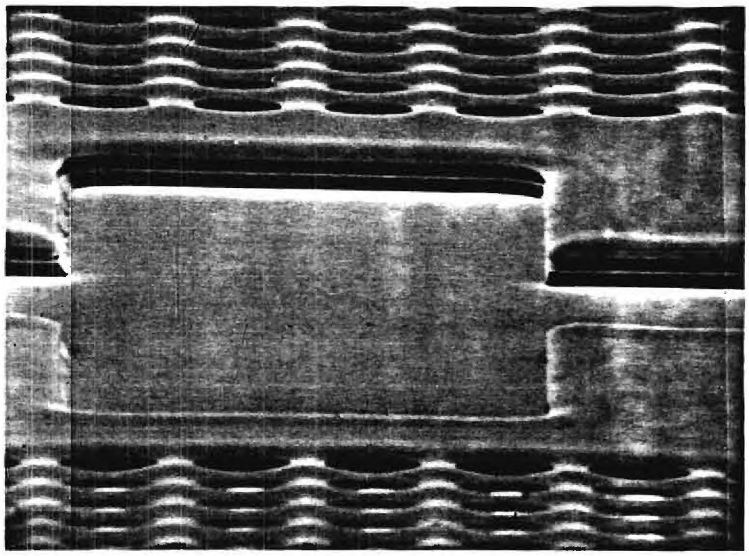


Figure 6. Same Pattern as Figure 5, but rotated 180°.

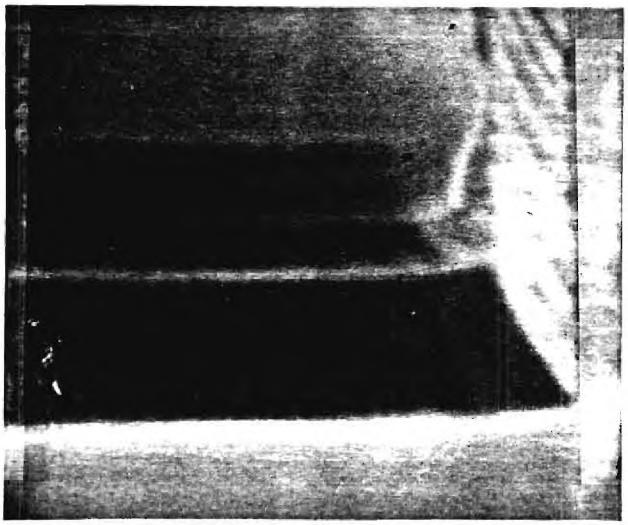


Figure 7. Close-up of SiO_2-PR Structure on left side.

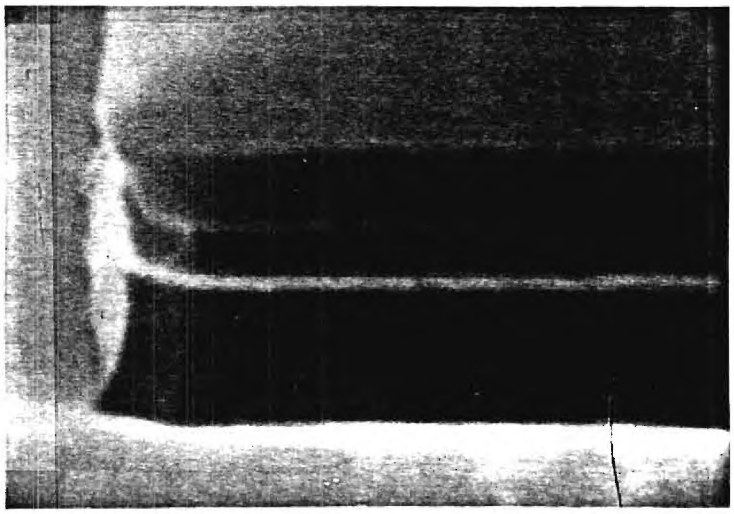


Figure 8. Close-up of SiO_2-PR structure on right side.

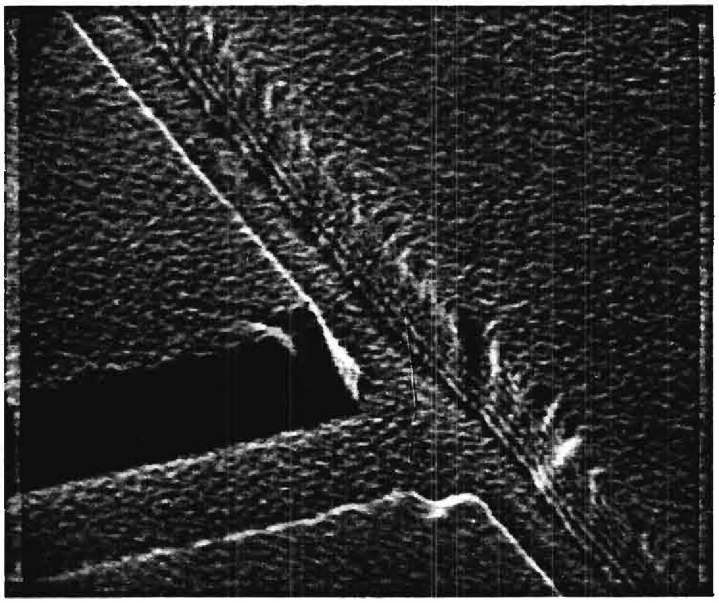


Figure 9. Shallow UV Resultant Pattern.

Del. No. 15

Status Report 7

LOW NOISE GaAs FET - PHASE II

CONTRACT PERIOD COVERED
1 JULY 1983 THROUGH 31 JULY 1983
P.O. S8-879406-LPY

A-3459

Submitted To
Hughes Aircraft Company
El Segundo, California 90234

by
Physical Sciences Division
Electromagnetics Laboratory
Engineering Experiment Station
Georgia Institute of Technology
Atlanta, Georgia 30332

Contracting through
Georgia Tech Research Institute
Georgia Institute of Technology
Atlanta, Georgia 30332

INTRODUCTION

This report describes the work performed on the program during the month of July. Penplots of the FET array mask set were reviewed and approved. W/Ti Schottky contacts were characterized and show good dc performance. Thick gate process development is continuing. Tests have been performed on DuPont polyimides and exposure optimization of AZ1350J photoresist has been completed.

TECHNICAL EFFORT

Contract Item 1- Design Mask Set

A CALMA data base tape was sent to Micro Mask Inc. on June 30. A purchase order from Hughes to Micro-Mask was received July 27 by Micro Mask. Penplots of all levels of the FET array were received August 1 and approved the same day. Delivery schedule for other items of the mask set design is as follows:

- Versatec Plots--8/8/83
- Films--8/22/83
- IX E-Beam Masters--8/24/83

Device fabrication should be started by the first of September if the above schedule is met.

Contract Item 6 - Develop Thick Gate Metal Process

As discussed in the previous monthly report, W/Ti metallization is being evaluated as a candidate for the Schottky contact metal in the thick gate process. Mixer diodes were fabricated on pieces

of GaAs wafer #8A501 which was used on the Hughes mixer diode program. W/Ti was sputter deposited at 50 watts with the substrate table continuously rotating. Gold was next deposited over the W/Ti to complete the Schottky contact.

Removal of the photoresist was accomplished by the tape lift-off technique. Substrates were thinned by mechanical lapping, and a AuGe-Ni-Au ohmic contact was evaporated on the back side of the wafer. The ohmic contact was alloyed at 450°C for 30 seconds in forming gas.

Two separate runs were made to check reproducibility. Eight diodes from the first run were electrically characterized. Ideality factors ranged from 1.13 to 1.23 and averaged 1.18. Figure 1 is an SEM photograph of diodes from this run. Figure 2 is a plot of the current-voltage characteristics of a typical diode. Figure 3 is a curve tracer photograph showing both forward

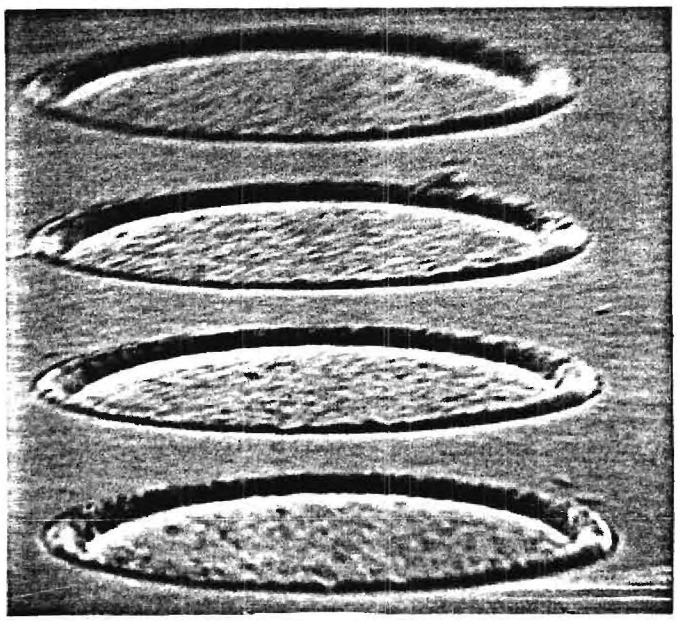


Figure 1. SEM of Mixer Diodes

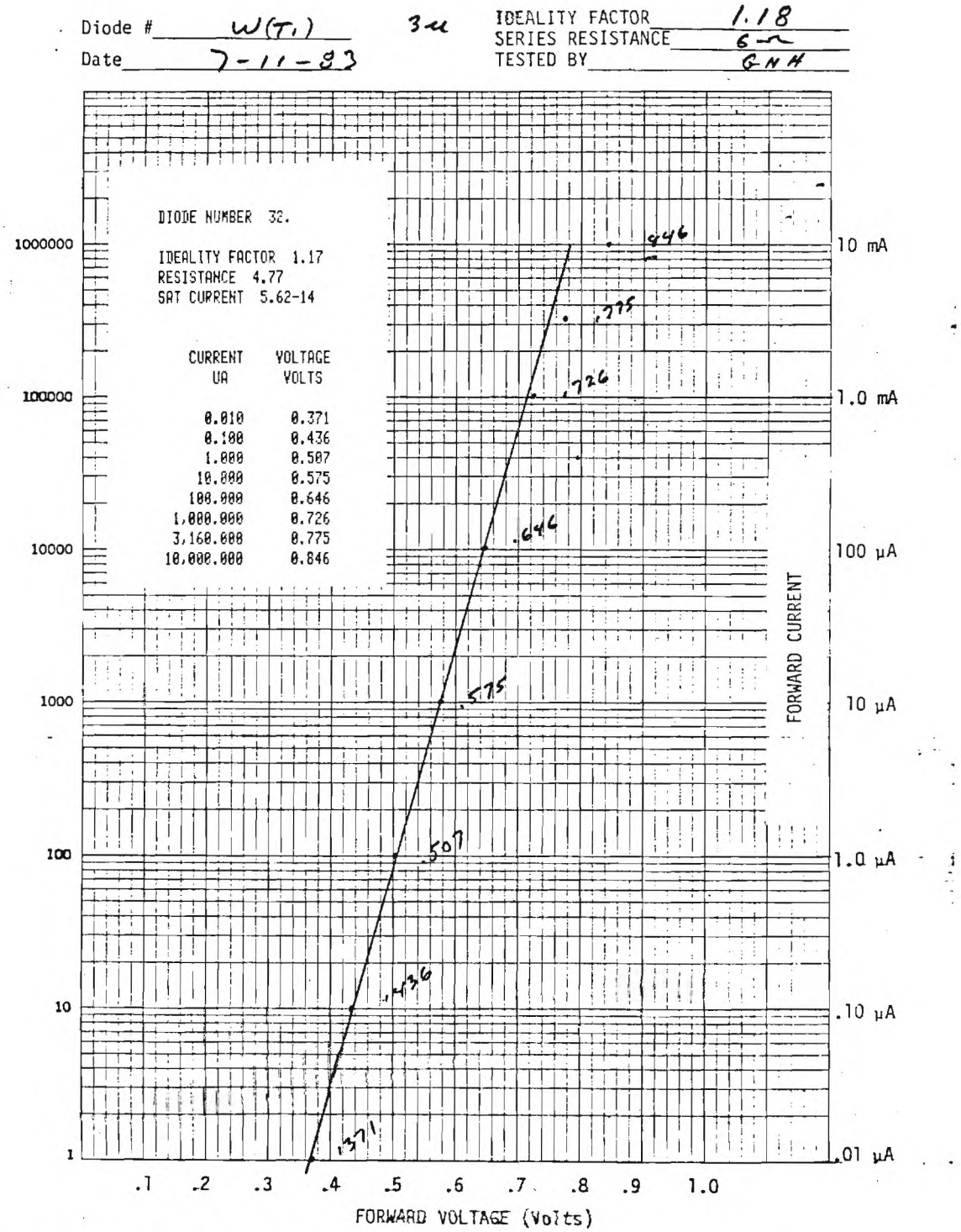


Figure 2. Current-Voltage Characteristics of First Run Diode

and reverse characteristics. DC electrical performance of these diodes is comparable to the E-beam evaporated devices.

Diodes from the second run had ideality factors ranging from 1.13 to 1.16 with an average value of 1.14. Eight diodes from this run were tested. Figure 4 shows the curve tracer signatures of a typical diode. Current-voltage characteristics are plotted in Figure 5.

Based on the results of these separate runs, it appears that W/Ti, deposited at low power by sputter deposition, is a suitable material for the Schottky gate contact. However, in addition to having good diode characteristics, the metal must be patternable. Due to sputter deposition with its excellent step coverage and the fact that electroplated gold over the sputtered metal is desirable, lift-off is not suitable for pattern delineation. As a result, a technique to etch the W/Ti is required.

Plasma etching of W/Ti with PDE-100 (a CF_4-O_2 mixture from LFE) was first attempted. Samples, which were plasma etched immediately after they had been deposited, etched well. However, samples which were subjected to gold etch solutions or chromic acid did not etch in PDE-100. Using a light plasma strip in O_2 prior to PDE-100 improved reproducibility; however, some areas were not completely cleared.

Discussions with personnel involved in plasma processing indicate that sulfur hexafluoride-oxygen mixtures are better suited to this application. A mixture of these gases has been ordered for evaluation.

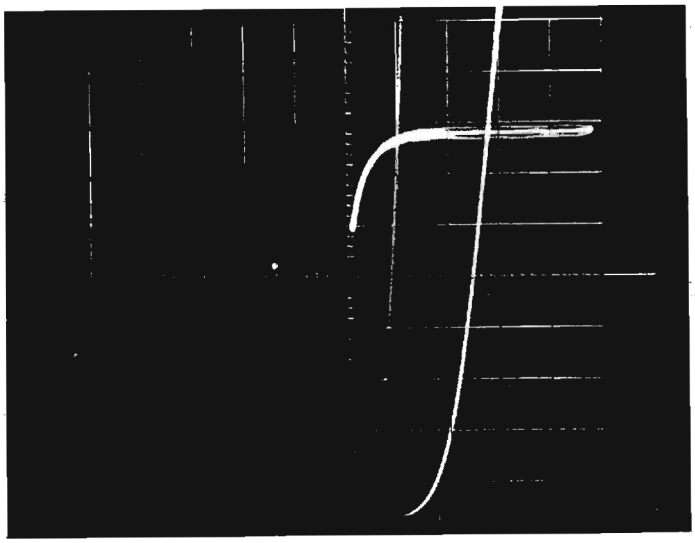


Figure 3. First Run Diodes Signatures

Upper Traces: Horiz. 2.0V/cm
Vert. 0.1ma /cm

Lower Traces: Horiz. 0.1V/cm
Left Vert. 0.01mA/cm
Right Vert. 1.0mA/cm

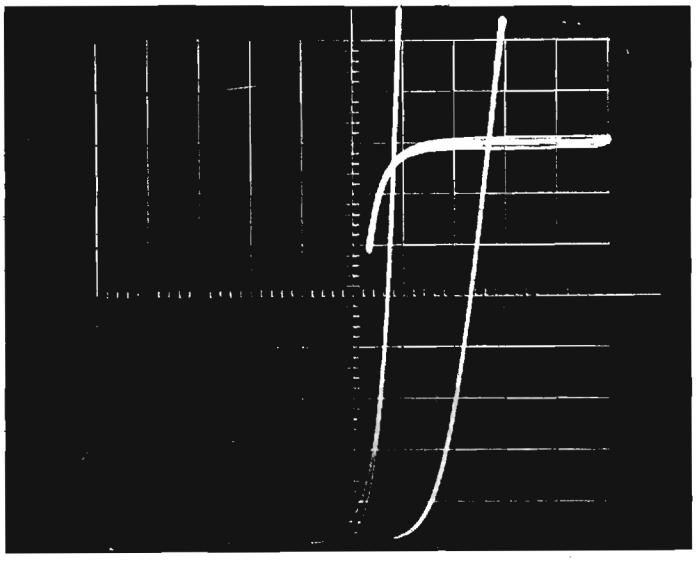


Figure 4. Second Run Diode Signatures

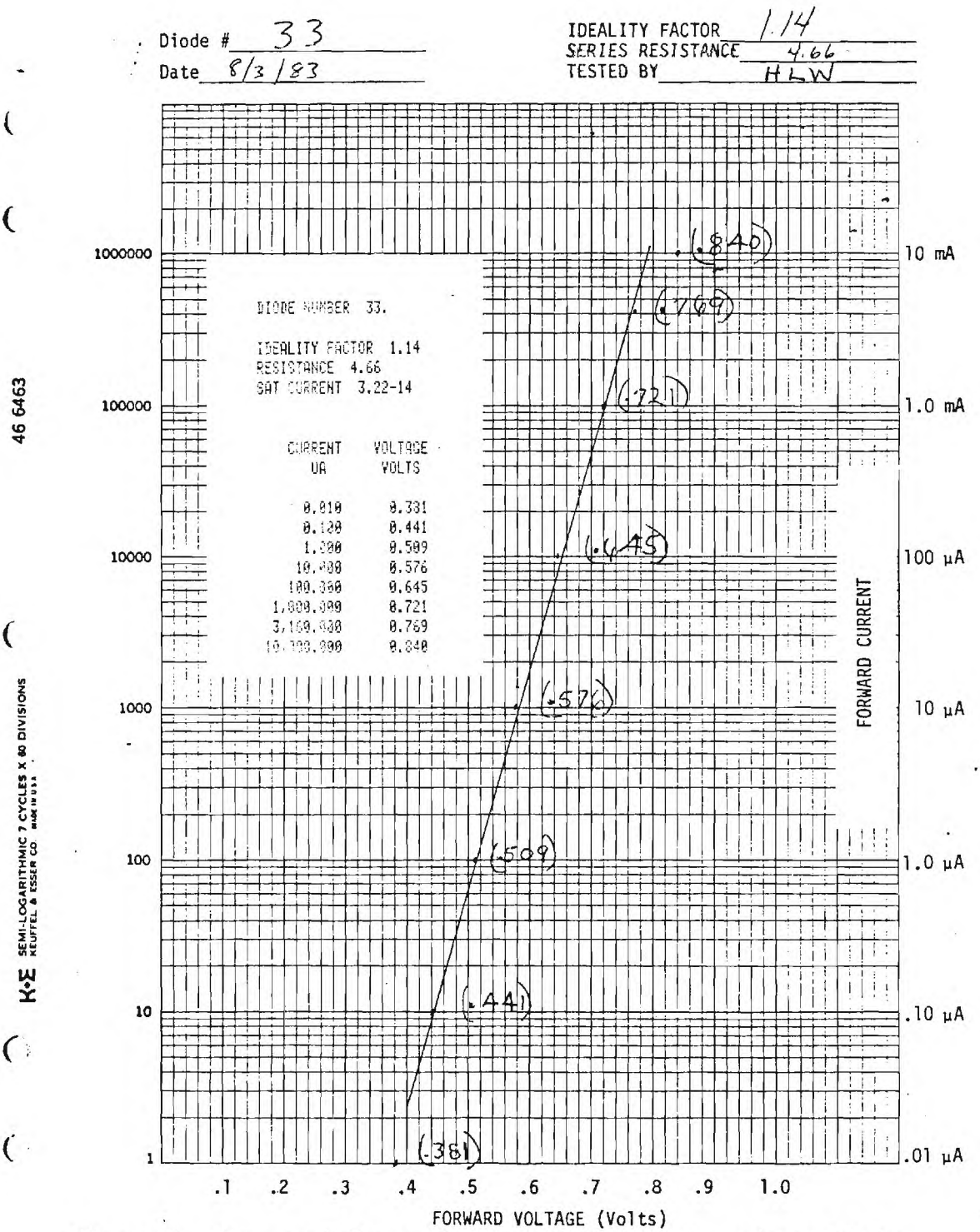


Figure 5. Current-Voltage Characteristics of Second Run Diode.

Wet chemical patterning of tungsten is also possible using mildly basic etching solutions [1]. This etchant containing

$34g\ KH_2\ PO_4$

$13.4g\ KOH$

$33g\ K_3Fe(CN)_6$

H_2O to make 1 liter

has a reported etch rate of = 1600 A/min. and is compatible with photoresist masks. Evaluation of this etchant to etch W/Ti is in progress. Other etches for tungsten are listed by Vossen and Kern [2].

Another aspect of the thick gate process which must be addressed is the procedure for gold electroplating. This procedure is equally important in the air bridge process. DC plating and periodic reverse plating are established procedures in this laboratory and have worked well in most applications. Air bridge structures, discussed last month, were made by periodic reverse plating. The structures were sound; however, surface finish was somewhat rough. Pulse plating is another method of electroplating which has been used to fabricate air bridge devices. This plating method is being evaluated in an effort to improve the plated gold surface finish.

Polyimide Tests

Nonuniformity in photoresist development was thought to be due in part to the non-planar surface geometry. Polyimide was evaluated in an effort to improve the photolithographic process yield. Test samples of DuPont's Pyralin polimide were obtained for evaluation. The products labeled PI-2550 and PI-2555 were processed according to manufacturer's specifications. Upon receipt, the polyimide coatings as well as their thinner were stored below 0°C. For evaluation, the polyimide coatings were loaded into hypodermic syringes. The PI-2550 was noted to be very thick at the time. According to the manufacturer, acetone is a solvent for the PI-2550. For this particular sample, this was not found to be true . A wafer coated with PI-2550 would not clean even after a 30 min. soak. PI-2550 was also found not to give uniform coating even after HMDS was used prior to coating. Thinning with the thinner provided did not improve the results.

PI-2555 gave slightly better results. It too was noted to be thicker than expected but it gave a good uniform coating (based on a visual inspection). After curing at 95°C for 1 hour, photoresist was applied, softbaked, and exposed. Since the polyimide etches in photoresist developer, it was etched at the same time the photoresist was developed. After developing for 45 seconds, the polyimide was found to have greatly undercut the photoresist. The etch rate of the polyimide is probably much more than the photoresist.

Since polyimide coating was not considered essential to the success of this program, further tests were not performed. However, the polyimide coatings are thought to have potential in applications where a dielectric is needed.

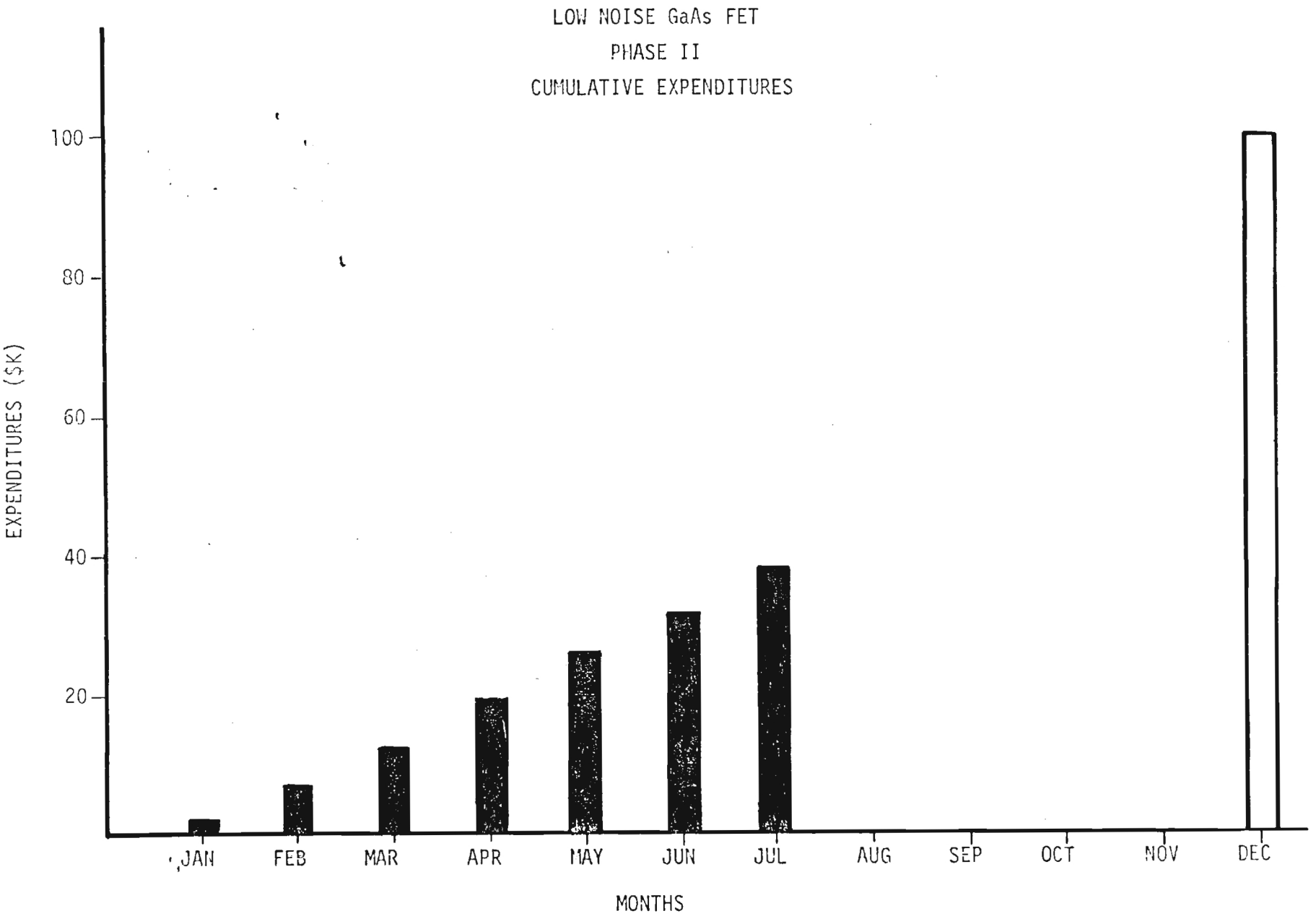
PLANS FOR NEXT MONTH

- Continue thick gate process
- Follow up on mask fabrication
- Evaluate pulse plating
- Evaluate ohmic contact process

REFERENCES

(1) T. A. Shankoff and E. A. Chandross, "High Resolution Tungsten Patterning Using Buffered, Mildly Basic Etching Solutions," J. Electrochem. Soc. 122, 294 (1975).

(2) J. L. Vossen and W. Kern, Thin Film Processes, Academic Press, New York, New York (1978).


LOW NOISE GaAs FET
PHASE II
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EXPENDITURES ($K)
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JAN
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DEC
MONTHS

Del No. 16

Status Report 8

LOW NOISE GaAs FET - PHASE II

CONTRACT PERIOD COVERED
1 August 1983 through 31 August 1983
P.O. S8-879406-LPY

A-3459

Submitted To
Hughes Aircraft Company
El Segundo, California 90234

by
Physical Sciences Division
Electromagnetics Laboratory
Engineering Experiment Station
Georgia Institute of Technology
Atlanta, Georgia 30332

Contracting through
Georgia Tech Research Institute
Georgia Institute of Technology
Atlanta, Georgia 30332

September 9, 1983

INTRODUCTION

This report describes the work performed on the program during the month of August. Versatec plots of the FET array mask set were reviewed and approved after modifications to one level. Thick gate process development has continued and is suitable for evaluation runs when the mask set arrives. Preliminary contact resistance tests have been performed using an in-house mask set.

TECHNICAL EFFORT

Contract Item 1 - Design Mask Set

Mebes format data has been generated by Micro Mask Inc. from the Calma data base tape prepared by Ga. Tech. Verstec plots (plots generated from the Mebes data) were received on August 10. These plots were incorrect because one dimension was plotted at 2733.5 microns rather than the actual 3733.5 microns. As a result, only part of the FET array pattern was plotted. Full size plots were received on August 18; however, level 4 was incorrect. Diagnostic structures in the center of the array were blank. A review of the penplots disclosed an extraneous boundary around the diagnostic pattern. Removal of the boundary resulted in the proper Verstec plot which was received and approved on August 25. As a result of these delays, scheduled delivery of the remaining items of the mask set design is as follows:

- Films - 9/9/83
- Ohmic mask - 9/2/83
- Mesa mask - 9/8/83
- Wide Gate mask - 9/8/83
- Narrow gate mask - 9/8/83
- Plated gate mask - 9/12/83
- Via mask - 9/12/83
- Air bridge mask - 9/12/83.

Run-out tests will be performed as soon as the mask set is delivered. Silicon wafers will be used for these tests.

Contract Item 6 - Develop Thick Gate Metal Process

Fabrication steps involved in the thick gate process include:

1. HMDS - 30 sec soak, spin 6000 RPM 25 sec.
2. Photoresist - 1350J 3:1, 6000 RPM 25 sec.
3. Softbake - 95°C 25 min.
4. Expose - 30 sec., 310 nm, 12.5mW/cm^2
5. Develop - microposit 351 3 1/2:1 45 sec.
6. Inspect -
7. Postbake - 110°C 10 min.
8. Plasma descum - 100 W 1 min.
9. Channel etch - monitor I_{dss}
10. Sputter deposit - substrate insulated from table
    W/Ti - 1000Å 75 W.
    Au - 2000Å
11. HMDS -
12. Photoresist - 1350J Neat 5000 RPM 25 sec.
13. Softbake - 95°C 25 min.
14. Expose - 3 min. 310 nm, 12.5 mW/cm^2
15. Develop - 45 sec.
16. Inspect -
17. Post bake - 110°C 10 min.
18. Plate Gold -
19. Remove Resist - Acetone
20. Etch thin gold - techni-strip
21. Etch W/Ti -
22. Remove Resist - Acetone/plasma.

Two areas of this process of particular concern are gold electroplating and W/Ti patterning.

Figure 1 is an SEM microphotograph of a plated gate structure basically prepared by the above procedure. A plated gate mask was not available. Gold plating was accomplished by periodic reverse plating at a relatively high current density. As seen in the photograph, the surface of the gold plating is rough. For submicron geometries, this amount of roughness may cause problems. As a result, pulse plating experiments were initiated. Sel Rex 401 Pur-A-Gold solution was employed. Pulse repetition rate was set at 100 msec., and 10% duty cycle was utilized. Various pulse amplitudes were employed, and some improvement was observed. However, none of the results, were significantly better than that obtained by normal dc plating. Figure 2 is an SEM of a gold plated layer 5 microns thick which was plated by dc plating procedures. A pulse plated sample of the same thickness is shown in figure 3. Air bridges made with this plating solution and the RFIC mask set are shown in figures 4 and 5.

Discussions with Sel Rex technical personnel resulted in the addition of cobalt nitrate to the solution as a grain refiner. Pulse plating and dc plating experiments with this solution showed no improvement in the grain structure.

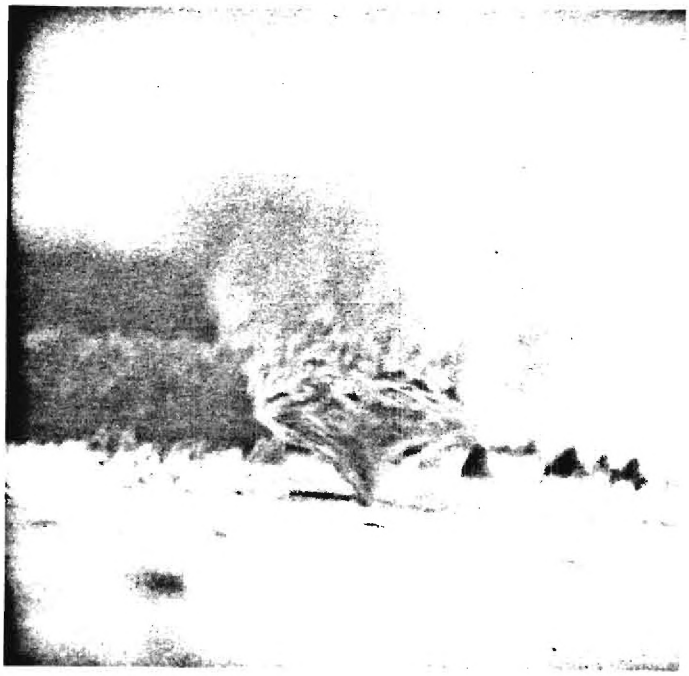
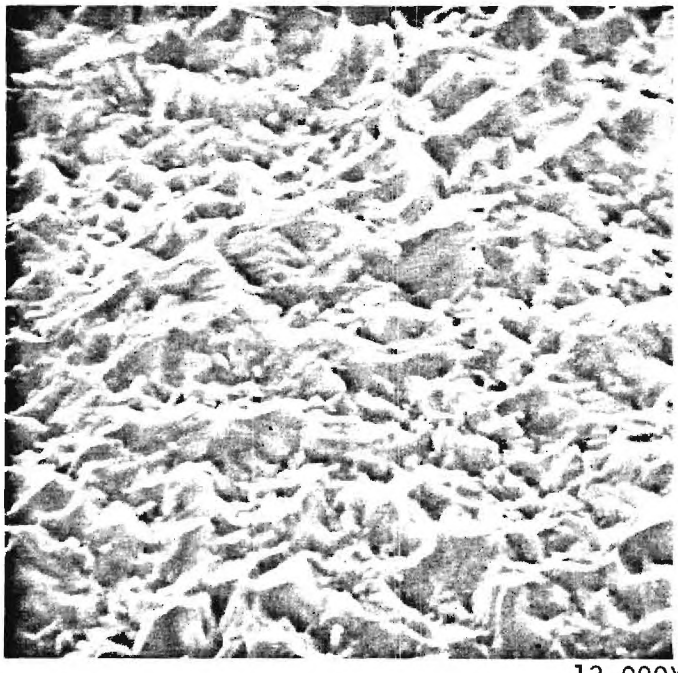


Figure 1. Plated Gate Structure.

These experiments indicated that small grain size is not readily attainable with the 401 solution. A phone call to Avantek Inc. disclosed that they were not using a pure gold (99.99%) solution. Due to company policy, other information was not available. In conversations with the sponsor, it was learned the Hughes uses BDT 510, an alkaline, noncyanide plating solution from Sel Rex. According to Sel Rex this solution must be used at a pH between 8.5 and 10. The alkaline nature of this solution may make it incompatible with positive photoresist. Shipley Company

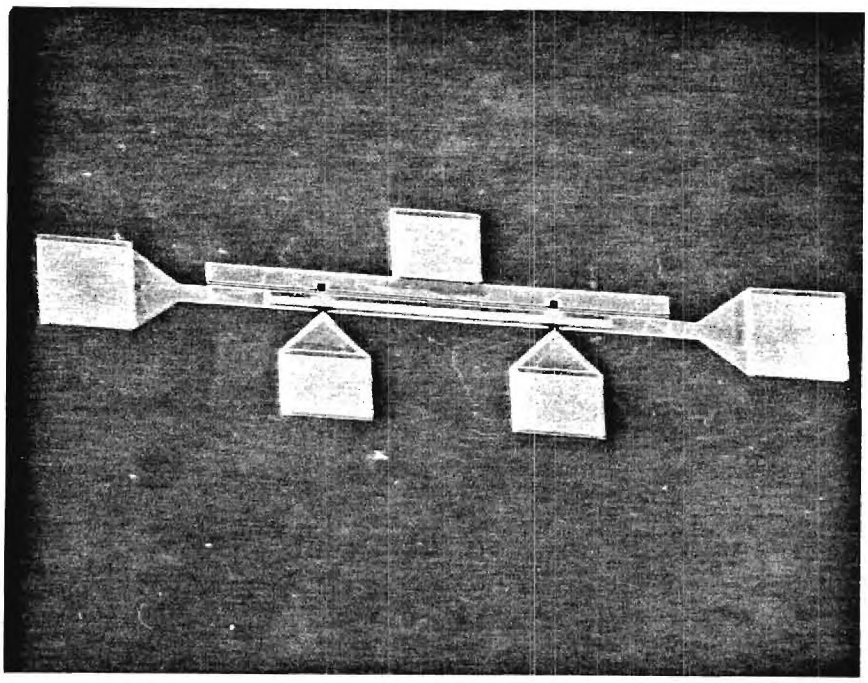
13,000X

Figure 2. DC Plated Gold



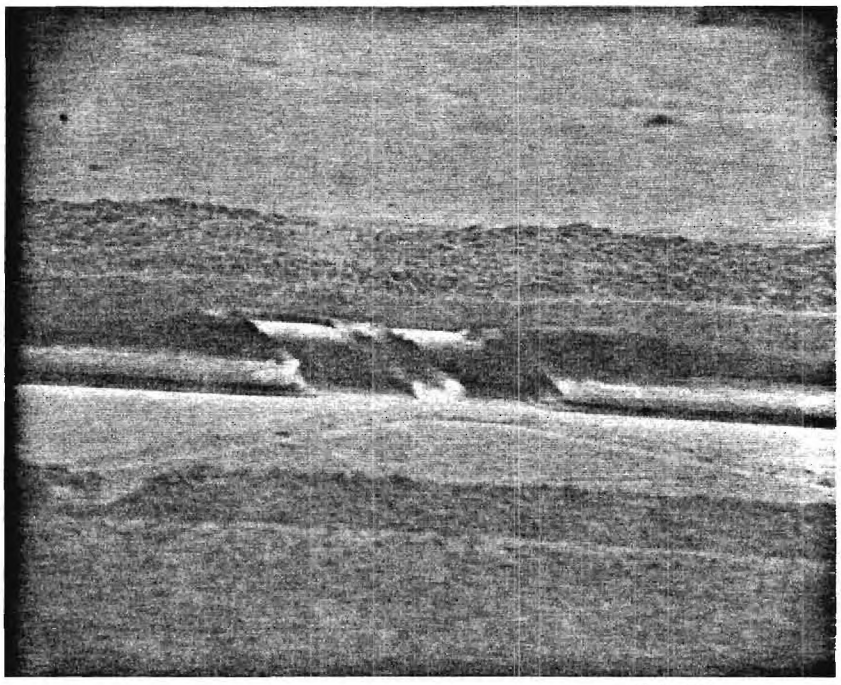
13,000X

Figure 3. Pulse Plated Gold



250X

Figure 4. RFIC FET Structure



5000X

Figure 5. Air Bridge

Inc. has been contacted for technical assistance concerning this matter, and literature has been requested from Sel Rex on the BDT 510 plating process. If, upon reviewing the literature, there is a reasonable chance that this plating solution is compatible with the other fabrication processes, it will be purchased and evaluated.

Tungsten/titanium, sputter deposited at low power, was found to provide a Schottky barrier contact with characteristics comparable to electron beam deposited Ti-Pt-Au. Pattern delineation of the W/Ti was of primary concern.

As reported last month, lift-off is not compatible with sputter deposition. Dry etching of W/Ti with PDE 100 can be performed but the results are inconsistent and depend on other processing steps prior to dry etching. Wet chemical etching, using a modified form of the mildly basic etching solution, has been evaluated and acceptable results have been obtained (1).

Tungsten etchant consisting of 34g. KH_2PO_4, 13.4g KOH, 33g $K_3Fe(CN)_6$ and H_2O to make one liter was prepared. Attempts to etch W/Ti with this solution were unsuccessful. Since this solution reportedly etches tungsten very well, it was concluded that a component was needed to etch the titanium.

A standard etchant for Ti consists of 9 parts H_2O to 1 part HF. A W/Ti etchant of 9 parts tungsten etch (described above) to 1 part HF was prepared. Tests performed on layers of W/Ti having a thickness on the order of 0.1 microns indicated that this etchant is effective in removing the W/Ti and is compatible with positive photoresist.

where R_{ij} and R_{jk} are the resistances between pads i and j and j and k, respectively, l_{ij} and l_{jk} are the distances separating the pads and W is the pad width in millimeters.

Two evaporation runs were made using GaAs material from the same wafer. An alloy time of 30 seconds was first used on each piece and the average contact resistance was .72 and .79 ohm-millimeters respectively. One wafer was subjected to an additional alloy of 3 minutes, and the average contact resistance was found to be .65 ohm-mm. Although run to run averages are reasonably consistent, pad to pad measurements varied over a wide range (.2 - 1.4 ohm-mm). It is clear from this evaluation, that small errors in the measurement of the distance between pads can cause large errors in the resultant contact resistance. Measurements made with the FET Array mask set should be more uniform and more accurate.

PLANS FOR NEXT MONTH

- Follow up on mask fabrication
- Finalize thick gate process
- Evaluate mask set for alignment
- Start device fabrication
- Evaluate SF_6

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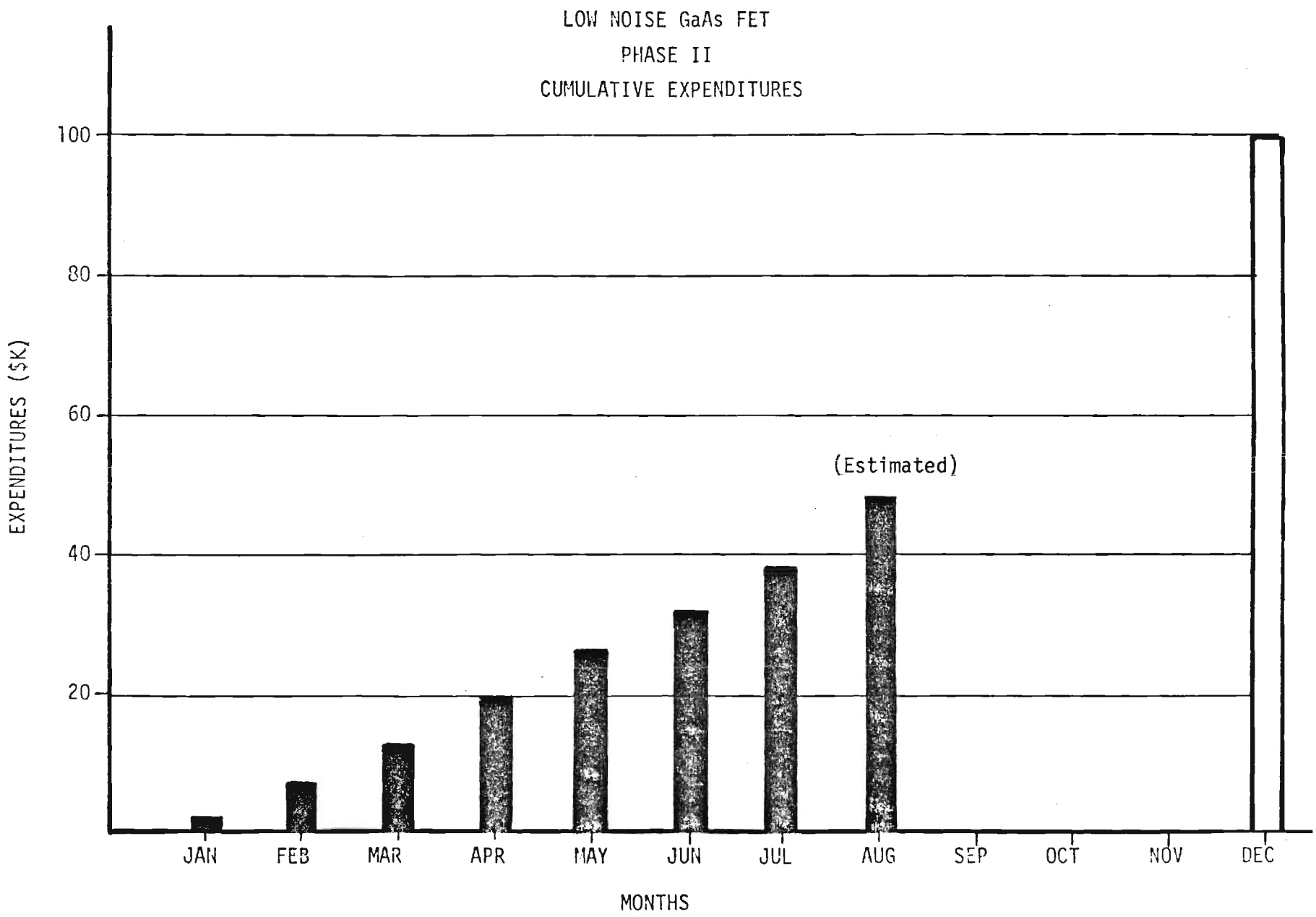
1. T.A. Shankoff and E.A. Chandross, "High Resolution Tungsten Patterning Using Buffered, Mildly Basic Etching Solutions," J. Electrochem. Soc. 122, 294 (1975).

2. A.A. Immorlica, Jr. etal. "A Diagnostic Pattern for GaAs FET Material Development and Process Monitoring," IEEE Trans. Electron Devices Vol. ED-27, pp. 2285-2291 Dec. 1980.

3. H.H. Berger, "Contact Resistance and Contact Resistivity," J. Electrochem. Soc., vol. 119, pp. 507-514, Apr. 1972.


LOW NOISE GaAs FET
PHASE II
CUMULATIVE EXPENDITURES
EXPENDITURES ($K)
100
80
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Del No. 18

Status Report 9

LOW NOISE GaAs FET - PHASE II

CONTRACT PERIOD COVERED
1 September 1983 through 30 September 1983
P.O. S8-879406-LPY

A-3459

Submitted To
Hughes Aircraft Company
El Segundo, California 90234

by
Physical Sciences Division
Electromagnetics Laboratory
Engineering Experiment Station
Georgia Institute of Technology
Atlanta, Georgia 30332

October 6, 1983

Gallium arsenide field effect transistors (GaAs FETs) have become the primary active components for X and Ku band low noise amplifier designs. In addition, monolithic analog microwave integrated circuits based on GaAs FET technology are becoming viable candidates for space and communications applications. Funded by Hughes Aircraft Space and Communications Group under P.O. number S8-879406-LPY, the Physical Sciences Division of the Georgia Tech Engineering Experiment Station has developed a monolithic compatible, high performance, low noise GaAs FET process. This research effort has involved the design and fabrication of a multi-layer mask set, specification and procurement of GaAs epitaxial material, submicron photolithography, Schottky barrier gate process development and the development of low loss crossover interconnections.

MASK SET DESIGN

Semiconductor process development requires an appropriate test vehicle. The most critical area of GaAs FET design is the Schottky barrier gate. If material quality and low contact resistances are maintained, gate length is the main factor in determining noise performance. Other factors considered important are gate resistance, gate to source spacing and gate recess. As a result of these considerations, computer modeling, and photolithographic capabilities; a mask set composed of an array of FETs was designed using the Georgia Tech Calma computer aided design system.

This test vehicle, shown in figure 1, contains 63 discrete FETs having gate lengths of 0.25, 0.50, 0.75 and 1.0 microns and various gate widths. A centrally located diagnostic pattern is also included within the array. Overall size of the array is 156 by 147 mils. Seven mask levels are utilized in this process and include:

Level #	Description
1	Ohmic Contact
2	Mesa
3	Wide Gate
4	Narrow Gate
5	Plated Gate
6	Vias
7	Air Bridge

Figure 2 is a plot of a discrete FET having a gate length of 0.25 microns and a gate width of 75 microns. Relationships of the various mask levels and design complexity can be seen in the plot.

Process and materials monitoring is necessary when developing a process as well as during production. The diagnostic pattern, shown in figure 1, is included for this purpose and contains:

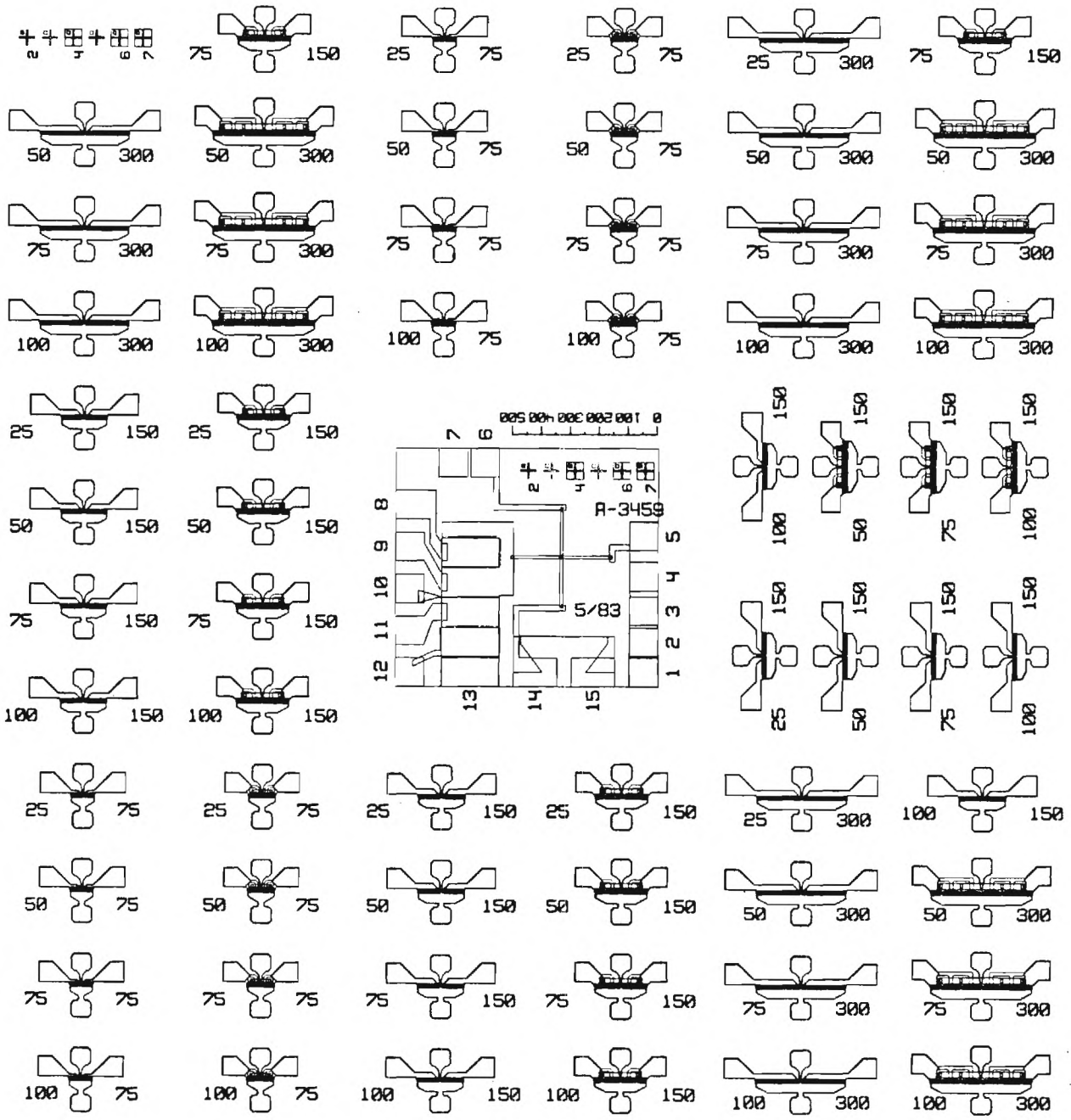


Figure 1. GaAs FET Array

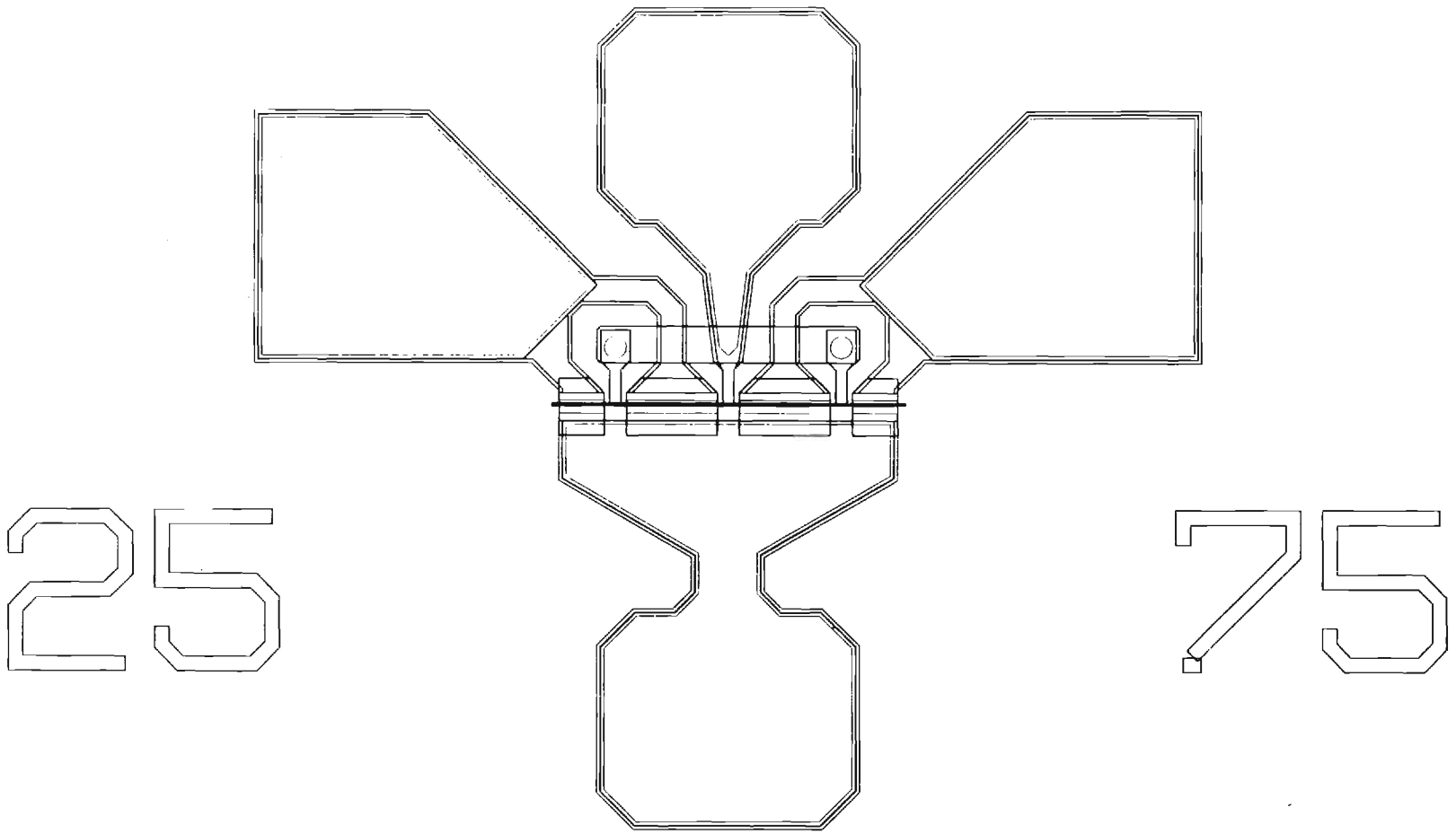


Figure 2. Discrete GaAs FET

Structure	Pad Numbers
Active Layer CV	8, 9
Isolation Test	6, 7
Greek Cross (for mobility measurements)	5, 6, 9, 14
One Micron (gate length) FET	9, 10, 11
Ohmic Contact	1, 2, 3, 4, 5
Gate Resistance	14, 15
FAT FET	11, 12, 13

MASK FABRICATION

Mask fabrication was performed by Micro Mask Inc. using a data base tape generated on the Georgia Tech Calma System. Since submicron geometries were required, direct writing of the pattern onto the mask using electron beam (E-beam) mask making equipment was specified. Current E-beam equipment is limited to a minimum spot size of 0.25 microns and a guaranteed minimum line width of 0.75 $\pm$ .25 microns. Micro Mask agreed to process this mask set on a best effort basis since the 0.25 and 0.50 micron geometries were below their guaranteed limits.

Data base information was converted to E-beam format and plots, generated from the E-beam formated data, were made to check for design or translation errors. After approval of the plots, 4" by 4" chrome masks were fabricated by Micro Mask. Gate lengths of 0.25 microns were not completely cleared on the masks;

however, other geometries were clear and near their designed size.

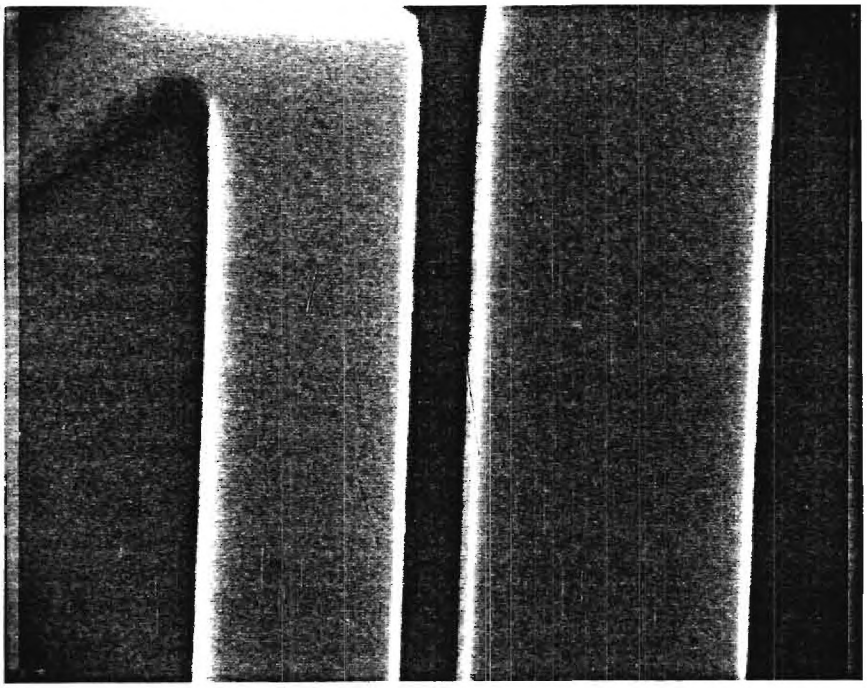
PHOTOLITHOGRAPHY

Delineation of the submicron geometries is one of the most important processing steps. A Karl Suss MJB3/HP submicron mask aligner was purchased for this research. Mid UV optics (310 nm) were installed, and the power supply was calibrated to provide a power density of 12.5 mW/cm^2.

Exposure and development tests were made to establish optimum conditions (1 to 1 replication of the mask pattern to the photoresist). Shipley AZ-1350J photoresist (thinned 3 to 1) was applied to test wafers and baked at 95°C for 25 minutes prior to exposure. Photoresist thickness was 0.7 microns as measured after development. Optimum conditions are dependent on the equipment and process techniques employed. For this process at Georgia Tech, an exposure energy of 250 mJ/cm^2 and a development time of 25 seconds (AZ 351 diluted 1 part to 3 1/2 parts H_2O) were optimum. Figure 3 is an SEM micrograph of a 0.50 micron gate pattern in photoresist at a magnification of 10,000 times. Edge acuity is excellent and the line length closely replicates the mask.

THICK GATE PROCESS

As the gate length decreases, the gate resistance increases to unacceptably high values unless provisions are made to modify the gate length to height aspect ratio or to permit multiple gate



10,000X

Figure 3. Submicron Photoresist Pattern

feeds. Level 5 of the mask set is included to provide an oversized, electroplated gold layer on top of the narrow Schottky gate metal defined by level 4.

Schottky contacts to GaAs using Ti-Pt-Au have provided excellent results on mixer diodes and FET gates patterned by a lift-off technique. Lift-off, in which the undesired metal is removed by desolving the underlying photoresist, requires that there be a break between the desired and undesired metal. As a result, lift-off is not compatible with electroplating.

Figure 4 is a cross sectional drawing of the characteristics of a lifted gate process and a plated gate process. In the lifted gate process, the gate metal cross-section becomes triangular due to closure of the photoresist opening during metal deposition. As gate lengths are reduced, this triangular gate structure results in high gate resistance.

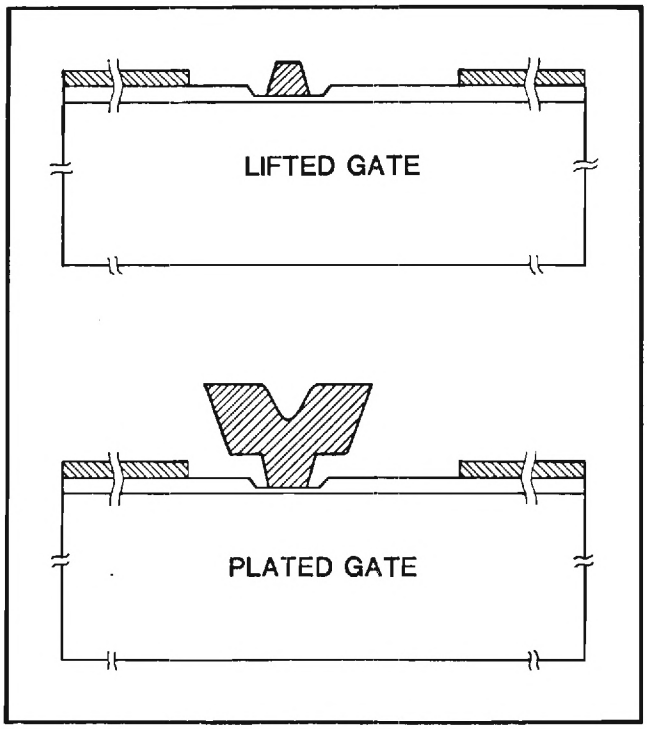


Figure 4. Gate Cross Sections

Low gate resistance is maintained in the plated gate process by the inclusion of thick plated gold on top of the narrow gate metal. This process requires an additional masking step and necessitates the use of narrow gate metals which can be easily

patterned by dry or wet chemical etching. Since platinum is difficult to etch, other metals were considered for the Schottky gate.

Tungsten/titanium (90%/10%) is a metal composition which has been used for Schottky contacts to GaAs. Evaluation of this metal was performed by fabricating mixer diodes on GaAs material known to given excellent results with Ti-Pt-Au contacts. DC electrical performance of the mixer diodes, having a W/Ti Schottky contact, was comparable to the Ti-Pt-Au Schottky mixers. Ideality factors of 1.14 were typically obtained on 3 micron diameter devices. Reverse breakdowns of greater than 6 volts were also noted.

In the plated gate process, removal of the excess W/Ti metallization must be performed by an etching process. Dry etching using sulfur hexafluoride is possible. A wet chemical etch to remove the W/Ti was also developed during this research. It consists of 9 parts tungsten etch, which contains:

34.0g KH_2PO_4

13.4g KOH

33.0g $K_3Fe(CN)_6$

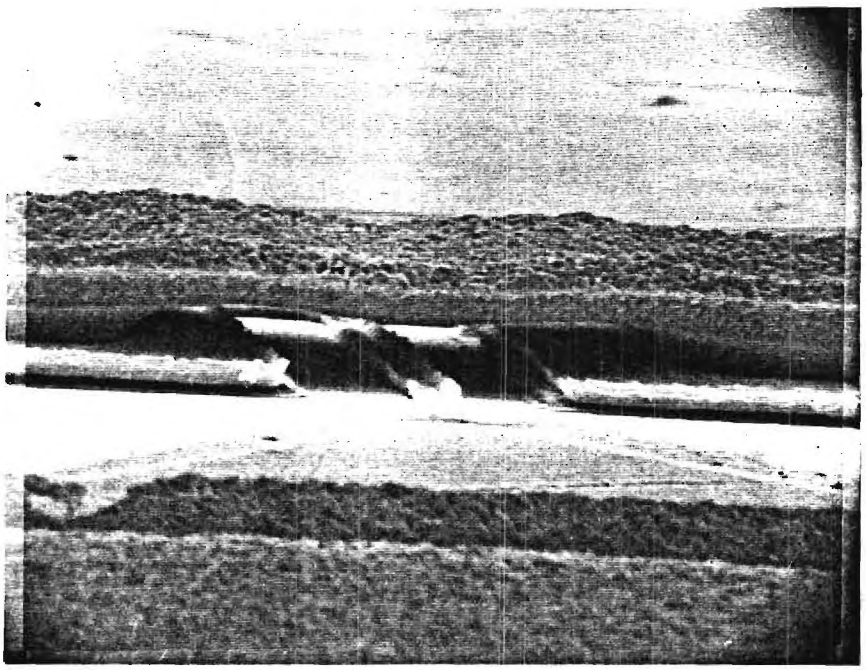
H_2O to make one liter,

to one part HF. This etchant is compatible with photoresist masks.

AIR BRIDGE PROCESS

Another technique to minimize the gate resistance is to use multiple gate feeds. Interconnection crossovers are required when

multiple gate feeds are used. A low loss air bridge crossover process was developed in this research to connect multiple gates to a common pad. Small openings called vias, which are centered over first level contact pads, are patterned in thick photoresist. Metal is evaporated over the entire wafer and another layer of photoresist is applied and patterned where the bridge is to be located. Gold is electroplated onto the regions where the evaporated metal is exposed. Solvents are used to remove the top layer of photoresist and the excess thin evaporated metal is chemically etched. Removal of the bottom layer of resist completes the process. Figure 5 is an SEM micrograph of a completed air bridge crossover.



5,000X

Figure 5. Air Bridge Crossover

SUMMARY

This research has addressed specific process development aspects required for reliable, high performance, low noise GaAs FETs. Fabrication of monolithic microwave integrated circuits utilizing the GaAs FET process of this research phase is a logical next step in the development of light weight, reliable space and communications circuits.

Del No. 20

Status Report 10

LOW NOISE GaAs FET - PHASE II

CONTRACT PERIOD COVERED
October 1983 through 31 October 1983
P.O. S8-879406-LPY

A-3459

Submitted to
Hughes Aircraft Company
El Segundo, California 90234

by
Physical Sciences Division
Electromagnetics Laboratory
Engineering Experiment Station
Georgia Institute of Technology
Atlanta, Georgia 3032

November 9, 1983

INTRODUCTION

This report describes the work performed on the program during the month of October. All levels of the mask set have been received and run-out tests have been performed on all critical levels. Level 5 of the mask set has been redesigned to correct initial design omissions. Improved electroplated gold layers have been obtained by the use of a new plating solution. Thick gate process development is continuing. The second GaAs FET wafer has been received from Raytheon.

TECHNICAL EFFFORT

Contract Item 1: Design Mask Set

All levels of the FET-ARRAY mask set, designed by Georgia Tech, have been received from Micro Mask Inc. Run-out tests on levels 1 through 5 using silicon wafers have shown acceptable alignment over a one inch diameter area. During the run-out tests, it was noted that there were minor design errors associated with the device identification numbers & diagnostic structure on level 5. Corrections to the Calma data base have been made and a tape has been forwarded to Micro Mask Inc. Wafer processing with the existing mask set is continuing since the errors do not affect the discrete FETs. Discussions with Micro Mask personnel indicated a two week turn around on the redesigned mask after they received the purchase order.

Contract Item 3. Procure GaAs Epitaxial Material

A second GaAs FET wafer has been received from Raytheon. As seen in Figure 1, the active layer has a concentration of 2 x 10^{17} cm^{-3} and has a thickness of 0.17 microns. This wafer utilizes a Cr doped substrate whereas the first wafer has an undoped substrate.

Contract Item 6: Develop Thick Gate Metal Process

Thick gate metal process development has focused on gold electroplating and removal of excess metal and photoresist after plating. As a result of discussions with the sponsor, Sel-Rex BDT 510 gold plating solution was purchased in an effort to improve the surface morphology of the plated gate. Figure 2 is an SEM micrograph of an electroplated air bridge structure fabricated with BDT 510. Comparing this metallization with Figure 5 of Status Report 8, it is seen that a much smaller grain size is obtained with the BDT 510 solution. Figure 3 is an SEM micrograph of the plated gate region showing the smooth gold plating. The thickness of the plating in Figure 3 is 1.75 microns. The use of 0.7 micron photoresist resulted in bridging of the gate and source metallization as seen in the figure. Even at this thickness, the metallization appearance is comparable to the Avantek M121 FET. Preliminary wire bonding tests on layers plated with BDT 510 showed no adhesion problems.

After gate metal electroplating, the excess sputtered metallization (W/Ti-Au) must be removed. The gold surface layer is easily removed with a commercially available gold stripper.

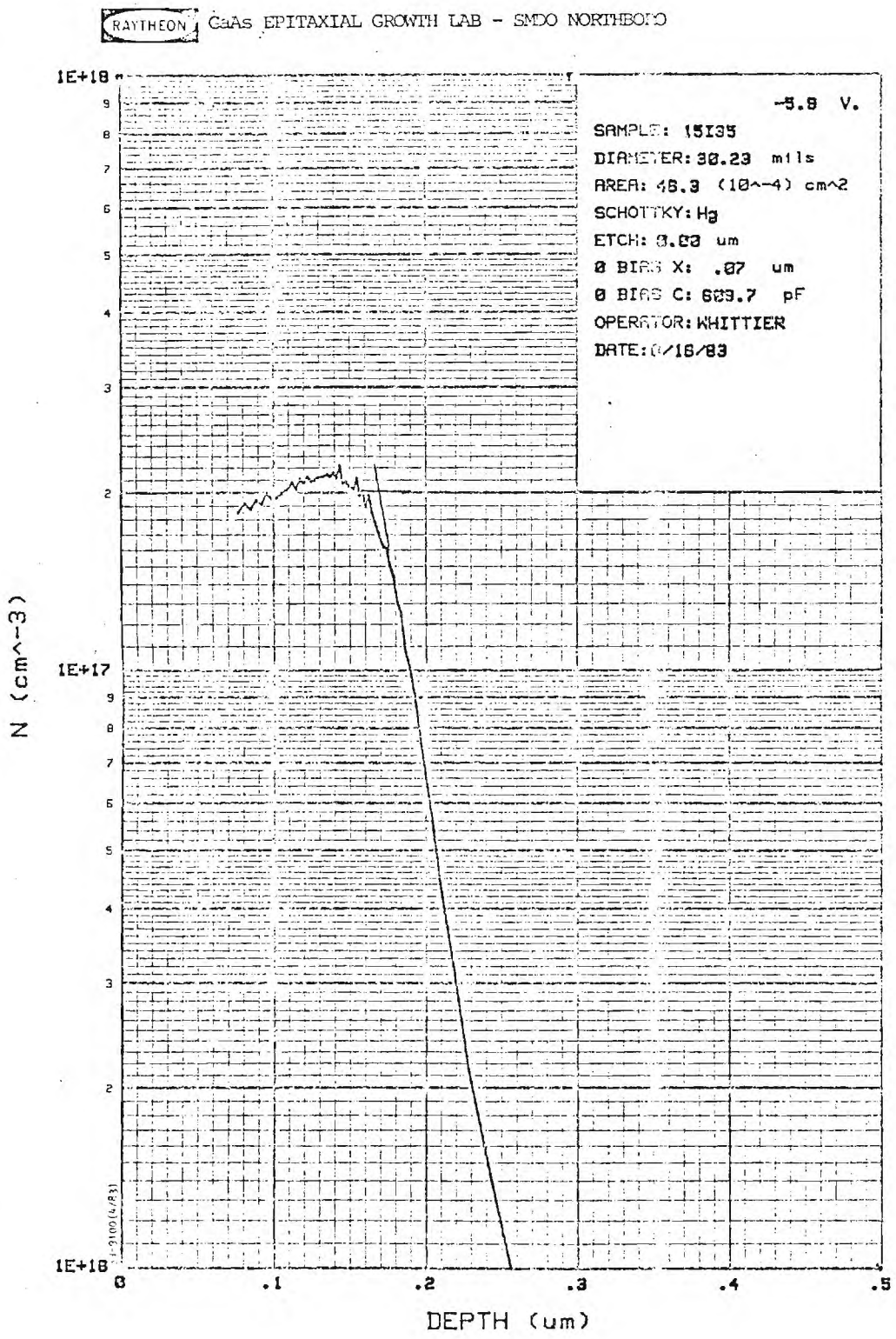
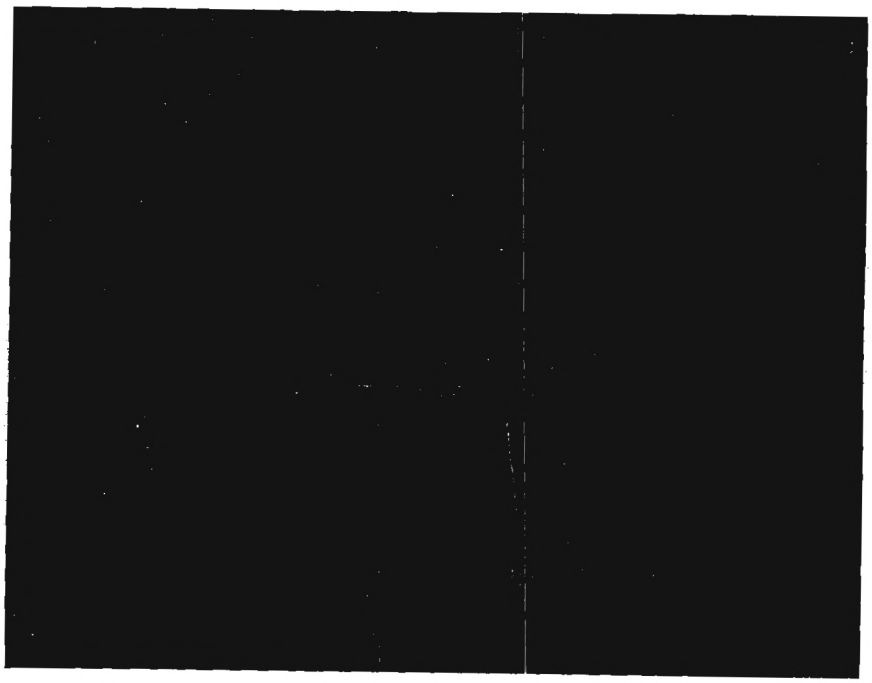
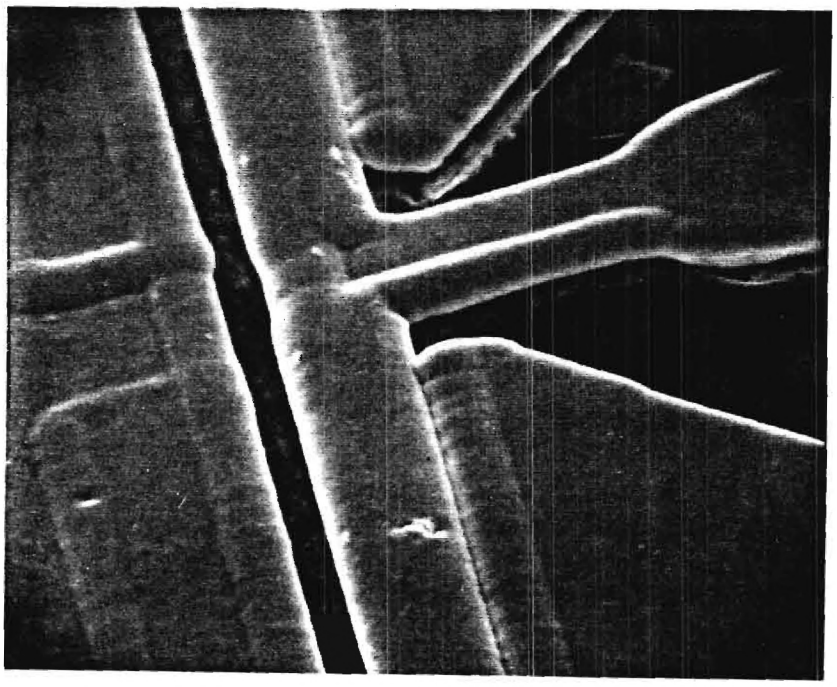


Figure 1. Active Layer Profile - GaAs Wafer # 2.



5000X

Figure 2. Air Bridge Plated with BDT 510.



5000X

Figure 3. Plated Gate Region.

The W/Ti is removed with the use of the etchant described in Status Report 8. However, removal of the bottom layer of photoresist has proved to be a problem. The interface layer between the photoresist and the W/Ti is altered during processing such that it cannot be removed by a simple acetone rinse. The acetone dissolves the underlying photoresist but does not affect the interface layer. Plasma removal of the layer is also ineffective as are commercial photoresist strippers. Per-sulfuric acid made by adding potassium persulfate to sulfuric acid appears to truly dissolve the interface layer (1). GaAs compatibility with this acid has not been performed to date. Additional work is still needed in this area to assure optimum results.

Sulfur hexafluoride was evaluated to determine if it could be used to plasma remove the W/Ti. These tests showed that the SF_6 would remove the W/Ti; however, it also attacks gold and, as a result, is not suitable in the thick gate process.

Contract Item 8 - Fabricate Test Devices

Fabrication of test devices has begun. Ohmic contact and mesa isolation is complete on the first wafer piece. Delivery of the first test devices is scheduled on or before November 23.

PLANS FOR NEXT MONTH

- Device Fabrication
- Receive new level 5 mask
- Evaluate ohmic contacts
- Order third GaAs wafer

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Del. No. 23

Status Report 11

LOW NOISE GaAs FET - PHASE II

CONTRACT PERIOD COVERED
1 November 1983 through 30 November 1983
P.O. S8-879406-LPY

A-3459

Submitted to
Hughes Aircraft Company
El Segundo, California 90234

by

Physical Sciences Division
Electromagnetics Laboratory
Engineering Experiment Station
Georgia Institute of Technology
Atlanta, Georgia 30332

December 10, 1983

INTRODUCTION

This report describes the work performed on the program during the month of November. The primary emphasis this month has been placed on fabrication of devices. Removal of the excess metal and associated photoresist is still a problem. One run of devices has been made using a lifted gate process in order to obtain information on the epitaxial material. Gate lengths were longer than expected, however, devices having a unity gain frequency in excess of 15 GHz were noted. Masks of the level 5 redesign have been received from Micro-mask.

TECHNICAL EFFORT

Contract Item 1: Design Mask Set

Masks of the level 5 redesign have been received from Micro-mask, but have not been checked for run-out. Visual inspection of the masks has disclosed that the specified corrections have been made. This redesign mask will be used on the next wafer run fabricated with the thick gate process.

Contract Item 3: Procure GaAs Epitaxial Material

Specifications for the third GaAs FET wafer are being completed. Due to mesa isolation, the active layer thickness must be kept small. An active layer thickness of 0.16 microns and a concentration on the order of 2.5 x 10^{17} cm^{-3} will probably be specified. Tighter tolerance on the doping tail will be discussed with Raytheon.

Contract Item 6: Develop Thick Gate Metal Process

Removal of the bottom layer of photoresist in the thick gate process

continues to be a problem area. Various procedures, including wet chemical and plasma techniques, have been evaluated to remove this photoresist. A combination plasma and wet chemical procedure has been found to work on test pieces prepared identically to the actual wafers. However, this procedure was not effective on an actual wafer run. Chemicals which appear to be effective in removing this photoresist are marginally compatible with the gate metal and/or the GaAs substrate. This problem has been discussed with the other staff members and much attention is being devoted to solving this problem.

Contract Item 8: Fabricate Test Devices

Five wafer runs have been processed to date. Four of these runs utilized the thick gate process and were aborted after trying to remove the photoresist described above. Wafer run number five was fabricated using a lifted gate process, and working devices were obtained. SEM analysis of this wafer run indicated that the gate lengths were longer than their designed values. Figure 1 shows a 0.5 micron device. The measured gate length is on the order of 1.0 micron rather than 0.5 microns. Although the gate lengths are larger than desired, gate definition is good as seen in the micrograph. The misalignment was deliberate in order to obtain devices having a 90 degree orientation with respect to the device shown. On subsequent runs, tweaking the photoresist process will make the misalignment unnecessary as gate lengths are brought closer to their designed values.

Figure 2 is a curve tracer photograph of a 0.5 micron long, 75 micron wide device. Point by point measurements of transconductance and gate capacitance have shown this device to have a maximum unity gain frequency of 15.2 GHz at a gate bias of 0.75 volts. Figure 3 shows the forward I-V

characteristic of the Schottky gate diode. Figure 4 shows the reverse characteristic and indicates minimal leakage current at gate voltages up to 5 volts. Measurement of the isolation between adjacent FETs has shown appreciable leakage current. This current, which is not controlled by the gate, decreases the transconductance and increases the device pinch-off voltage (V_p at 1 mA is typically 2.5 volts for a 0.75 by 150 micron FET on this wafer). A longer mesa etch is expected to eliminate this problem.

PLANS FOR NEXT MONTH

- Device Fabrication
- Deliver Test Devices
- Evaluate Drift Mobility
- Begin Final Report Documentation

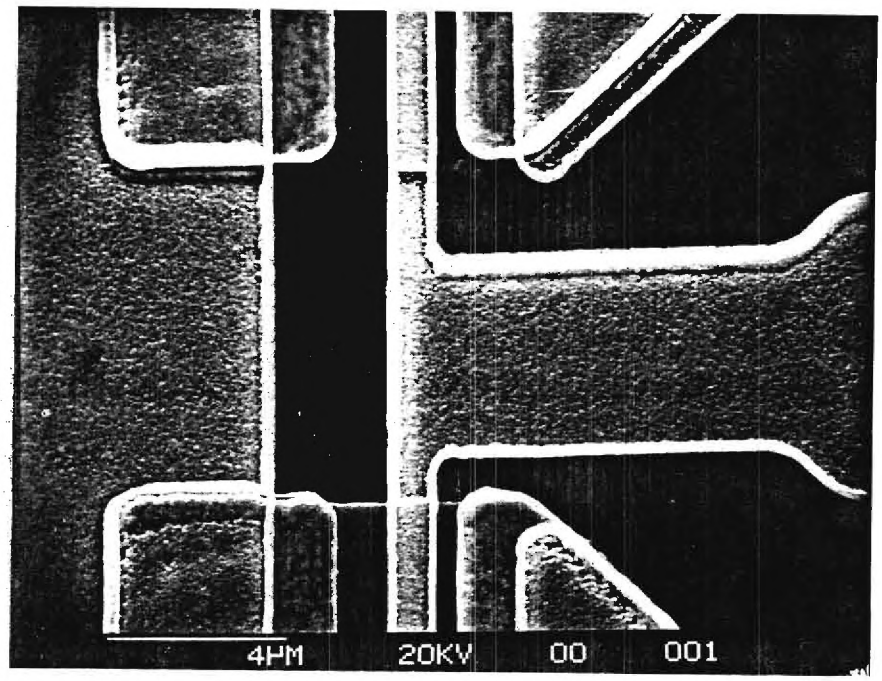

Figure 1. Gate Region - 0.5 x 150 Micron Device

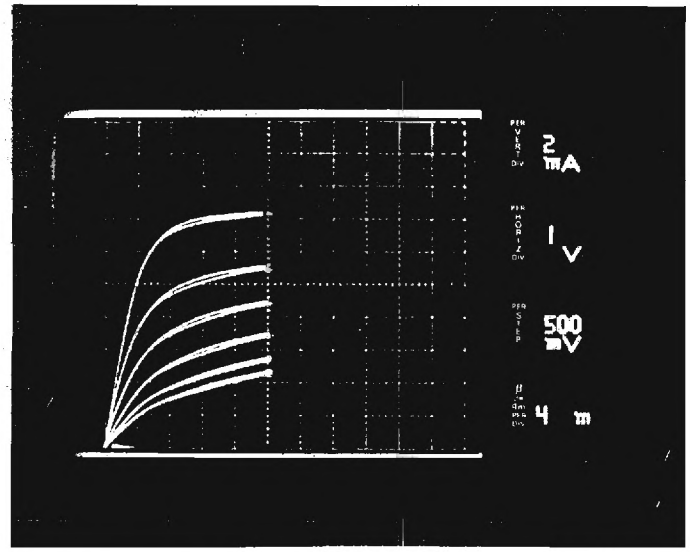

Figure 2. I-V Characteristics - 0.5 x 75 Micron Device

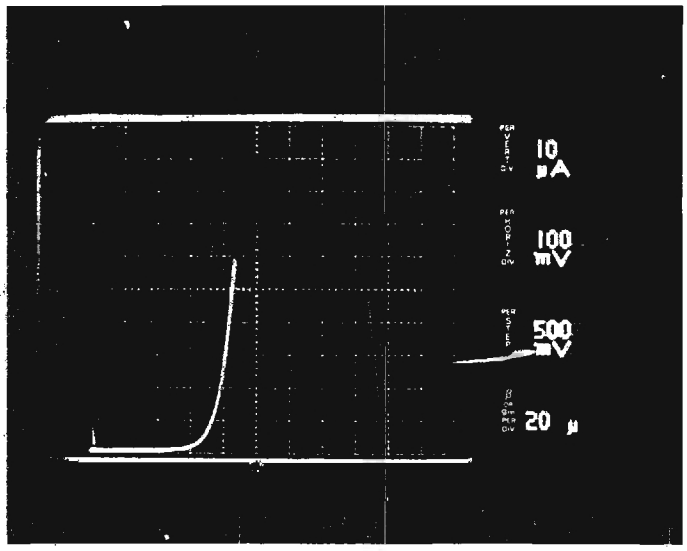

Figure 3. Gate Forward I-V Characteristic

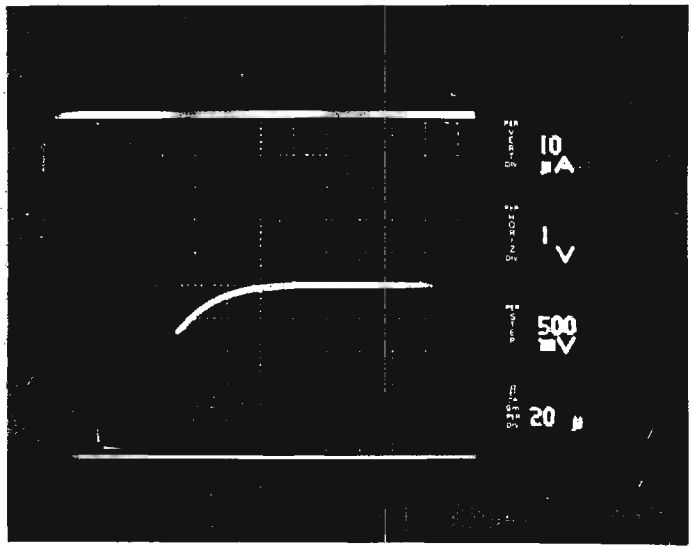

Figure 4. Gate Reverse I-V Characteristic

Del No. 26

Status Report 12

LOW NOISE GaAs FET - PHASE II

CONTRACT PERIOD COVERED
1 December 1983 through 31 December 1983
P.O. S8-879406-LPY

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Submitted to
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El Segundo, California 90234

by

Physical Sciences Division
Electromagnetics Laboratory
Engineering Experiment Station
Georgia Institute of Technology
Atlanta, Georgia 30332

January 23, 1984

INTRODUCTION

This report summarizes the work performed on the program during the month of December. Specific details will be discussed during the program review scheduled for February 3. Emphasis this month has been placed on device fabrication and delivery of test devices. Photoresist removal during the thick gate process continues to be a problem. Test devices fabricated with a lifted gate process were delivered for evaluation. Heat treatment after gate deposition has been shown to improve device I-V characteristics and the gate to source diode ideality factor. The third epitaxial wafer has been ordered.

TECHNICAL EFFORT

Contract Item - Procure GaAs Epitaxial Material

The third epitaxial wafer has been ordered from Raytheon. Based on the results obtained on the previous wafers, specifications for this wafer were determined. An active layer concentration of 2.5 x 1017 cm-3 was specified. This higher concentration should increase the device transconductance which has been approximately 100 ms/mm on the previous wafers. Active layer thickness was specified at 0.16 microns due to mesa isolation and pinch off voltage requirements. Tighter tolerance on the doping tail was discussed with Raytheon. A sharper transition from active layer concentration to buffer layer concentration can be obtained if the buffer layer thickness is kept small (on the order of one micron rather the two or three).

three). Delivery of this wafer will complete this contract item.

Contract Item 6 - Develop Thick Gate Process

Work is continuing on the thick gate process. Removal of the bottom resist layer is the problem area. An alternate process in which the wafer is first coated with photoresist and then coated with evaporated gold prior to any gate patterning has been evaluated. The evaporated gold was introduced to eliminate the apparent interface problem between the photoresist and sputtered metal.

Optimum sputtered metal thickness was not obtained due to an undetected change in the sputtering system table height. However, encouraging results were obtained. Removal of the bottom resist layer was easier although still incomplete. Working devices were obtained, and a transconductance of 133 ms/mm was noted on one device. However, 0.5 micron and some 0.75 micron devices were not clearly delineated prior to gate metal deposition. Additional evaluation of this alternate process might lead to successful resist removal.

Contract Item 8 - Fabricate Test Devices

Test devices fabricated with a lifted gate process have been delivered for evaluation. As discussed last month, gate lengths were larger than desired and, as a result, the unity gain frequency was lower than expected.

Additional testing of devices from this run has disclosed that improvement in transconductance and gate to source diode ideality factor can be obtained by heat treating after gate

deposition. Improvements on the order of 20% have been seen on ideality factors. Optimum heat treat conditions have not been determined; however, they will be established and incorporated into the standard process.

PLANS FOR NEXT MONTH

- Device Fabrication
- Deliver Additional Test Devices
- Prepare Program Review

Del No. 27-28

Status Report 13-14

LOW NOISE GaAs FET - PHASE II

Contract period covered
1 January 1984 through 9 March 1984
P.O. S8-879406-LPY

A-3459

Submitted to
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El Segundo, California 90234

by

Physical Sciences Division
Electromagnetics Laboratory
Engineering Experiment Station
Georgia Institute of Technology
Atlanta, Georgia 30332

March 16, 1984

INTRODUCTION

This report summarizes the work performed on the program during the months of January and February. Work during January was discussed at the program review February 3 and is included in this report for completeness. Emphasis this reporting period has been placed on removal of excess material at the gate step in the fabrication process. Other areas of progress include ohmic contact metallization and GaAs materials.

TECHNICAL EFFORT

Contract Item 2 - Define Mask Set

Seven levels comprise the mask set for this program. All levels except the narrow gate mask have critical dimensions greater than or equal to 0.75 microns. One quarter (0.25) micron gate lines were designed on the narrow gate mask; however, at the time of mask fabrication, Micro Mask Inc. as well as all other mask vendors contacted could not guarantee geometries under 0.75 microns. As a result, all the 0.25 and some 0.5 micron designed lines did not register on the narrow gate mask.

Recent discussions with Micro Mask personnel disclosed that they are in the process of installing a new E-beam mask making system. The new system will have a spot size on the order of 0.1 micron and should make it possible to print the 0.25 micron gate lines by rerunning the existing data base tape of the narrow gate

level. This system should be on line by May or June.

Contract Item 4 - Procure GaAs Epitaxial Material

The third epitaxial wafer has been received from Raytheon. A profile of this uniformly doped material, having an active layer concentration of 2.0×10^{17} cm^{-3} is shown in figure 1. This material has an active layer thickness of 0.16 microns and a buffer layer thickness of 2.5 microns.

This wafer was ordered prior to the program review in which a retrograde doping profile was discussed. Conversations with Raytheon personnel disclosed that they grow epitaxial layers with graded profiles. They indicated that they would send some samples along with profile information.

Technical articles concerning graded profiles for GaAs FET applications have been reviewed.[1-4] Calculations of the proper concentrations and thicknesses have not been completed; however, MBE growth capabilities have been located and layers will be grown when the specifications are completed.

Contract Item 6 - Develop Thick Gate Process

As discussed during the program review, removal of the excess metal and the bottom photoresist layer is the major problem area of the fabrication process. The use of an oxide in lieu of the bottom resist layer was discussed at the program review. Efforts on this task have focused on oxide deposition and patterning as well as removal of the thin metal deposited on the oxide.

Oxide deposition was performed in the CVD reactor used on

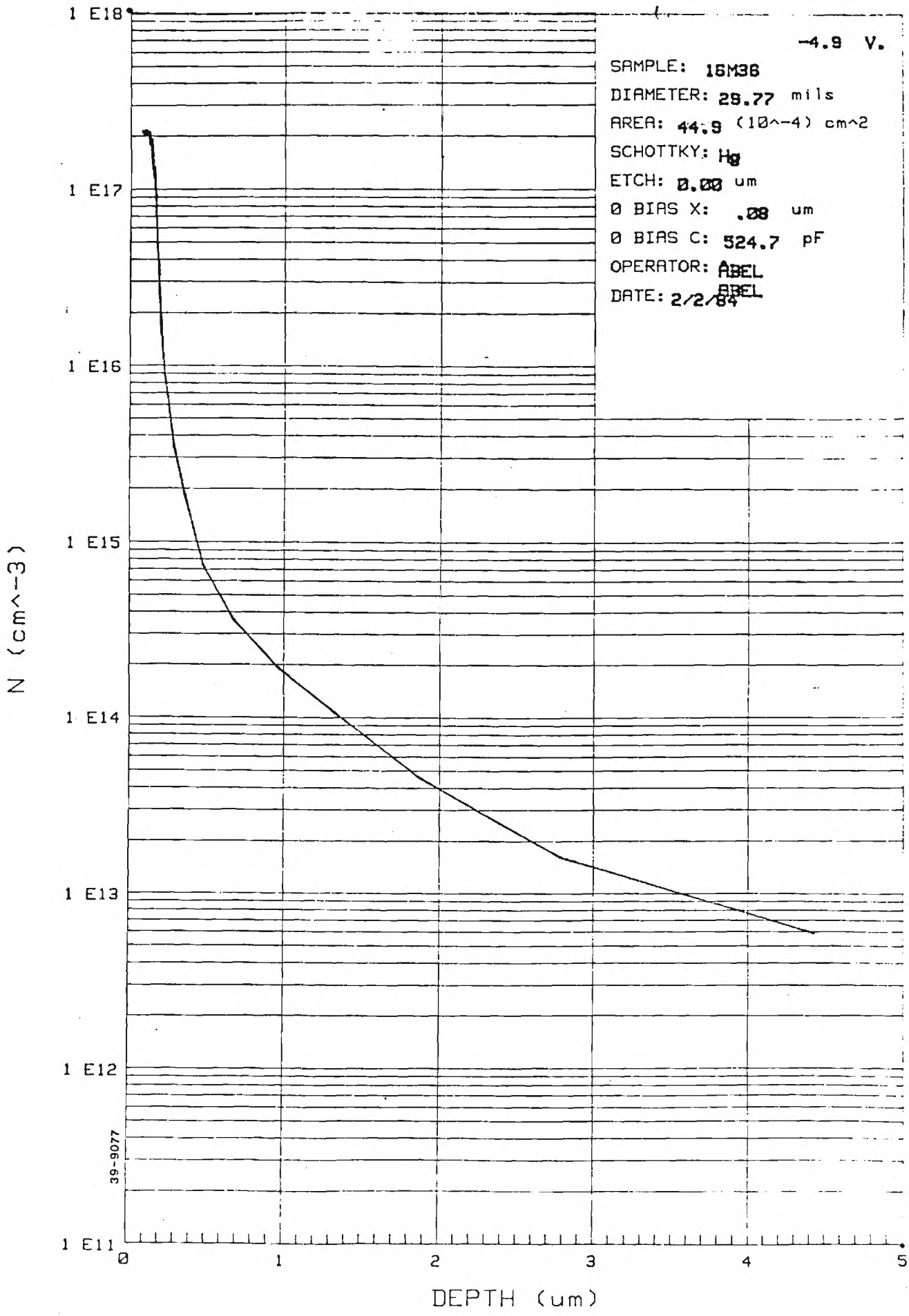
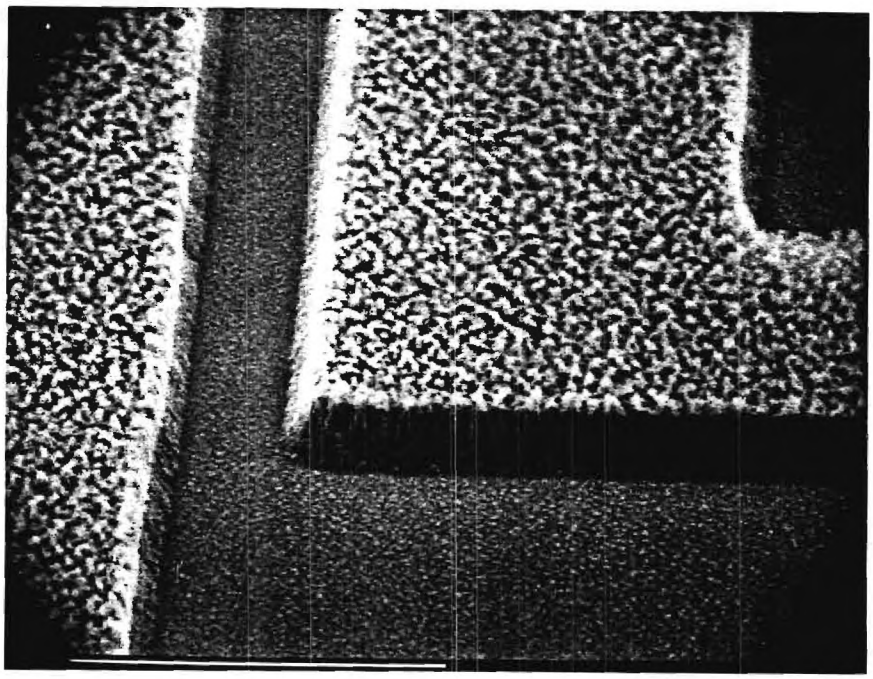


Figure 1. Wafer Three Doping Profile.

the mixer diode program.[5] A 1000 Å layer was deposited after the mesa isolation step. A 6000 Å photoresist layer was applied, and the wafer was patterned in the conventional manner. Wet chemical etching, using buffered HF, resulted in undercutting and excessively large gate lengths. Planar plasma etching was next evaluated as a means of delineating the pattern with minimal isotropic etch.

A Technics PEIIA planar plasma etcher, using LFE PDE 100 (CF_4 - O_2) gas, was used to etch the oxide. Test pieces were coated with oxide and patterned with resist. Plasma tests, using various pressure, power and time variations, were performed. Best results were obtained at 50 watts for 20 minutes with a chamber pressure of 200 mTorr. Figure 2 is an SEM micrograph of a 0.5 micron gate line etched in this manner. As seen in the micrograph, the oxide opening is very near the desired 0.5 micron dimension. Photoresist covers the unetched region in the micrograph and the plasma effects on the resist are clearly seen. Even though the plasma erroded the resist, removal of the remaining resist was easily accomplished with an acetone rinse.



26,000X

Figure 2. Gate Pattern in Oxide.

Schottky gate metal was sputter deposited at 50 watts. The gate region was then plated with gold (7000 Å). Removal of the top layer of resist was accomplished by an acetone soak followed by a 1 minute soak in μ posit 140.

The wafer was divided into four regions using black wax, and different procedures were used to remove the thin metal. On the first quadrant, the gold was removed with Techni-strip gold etchant. W/Ti removal was attempted with the KH_2PO_4 solution

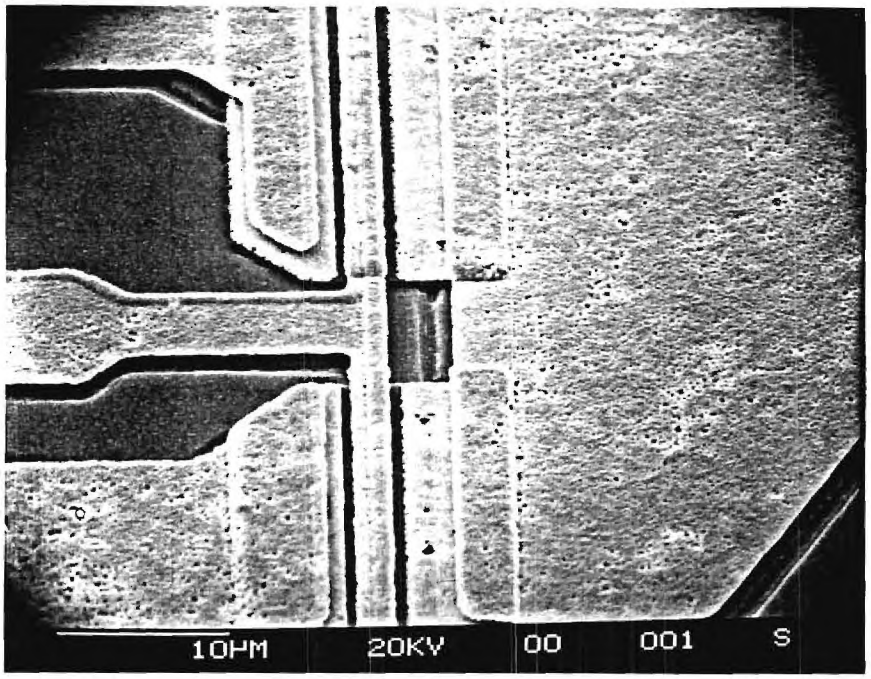
described in previous reports. Incomplete removal of the W/Ti was noted in some areas and undercutting of the gate metal was observed in other areas. Further tests indicated that this etchant also attacks GaAs.

The second quadrant was etched with dilute aqua regia to remove the gold. A (CF_4-O_2) plasma was used to etch the W/Ti in combination with wet chemical etching using H_2O_2. SEM analysis disclosed excessive etching of the GaAs at the pattern edges. Probable cause of the etching was the aqua regia etch used to remove the gold.

After reviewing the literature on plasma etching of tungsten, attempts to remove the thin metal were made on quadrants three and four.[6-8] Plasma removal of the gold and W/Ti was attempted on quadrant three. Working devices were obtained; however, the saturated current was much lower than expected.

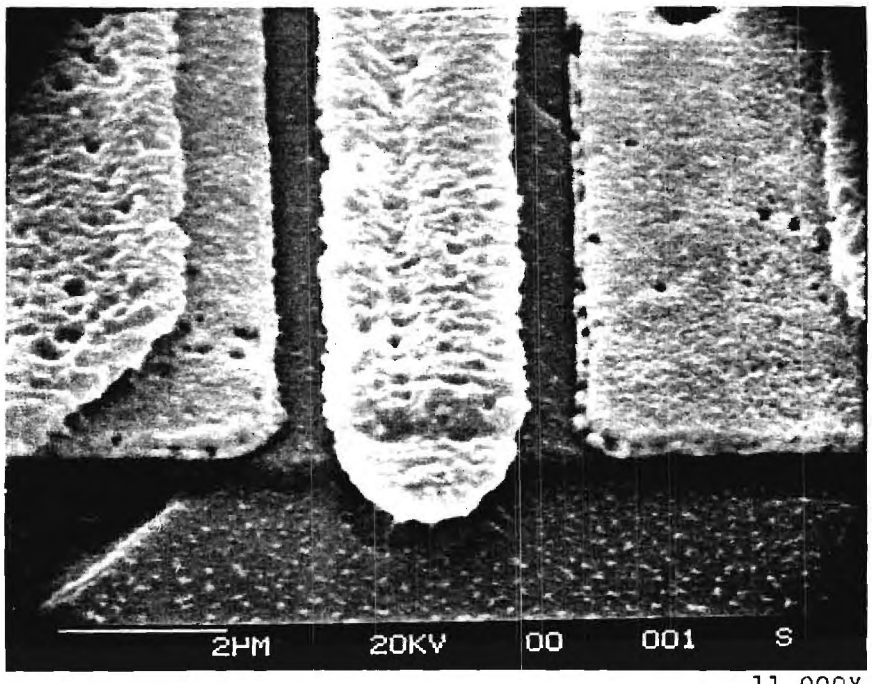
Removal of the gold layer on quadrant four was accomplished using a Film Microelectronics Inc. etchant (C35) at 35°C with sonic agitation. Plasma removal of the W/Ti layer was accomplished at a power level of 10W for 10 minutes at 60°C. A chamber pressure of 100 mTorr was used. Inspection of the wafer disclosed that most of the metal was removed. The same conditions were repeated in order to remove the underlying oxide. Buffered HF was used as a final clean-up etch.

SEM analysis of devices in quadrant four revealed well defined gate lines free of excess metal. Figures 3, 4 and 5 are



2,300X

Figure 3. Quadrant Four Device



11,000X

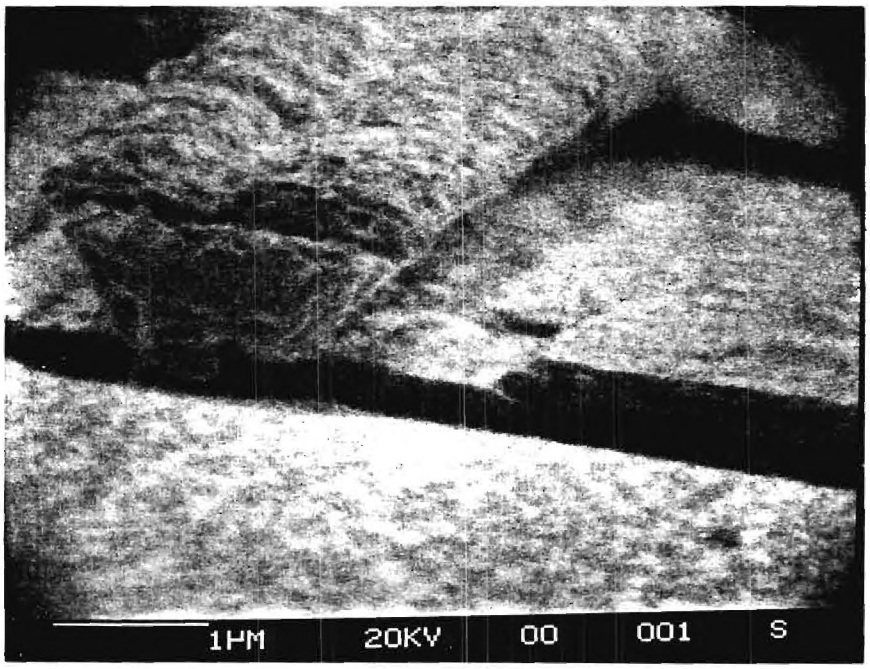
Figure 4. Gate Region

micrographs showing the gate region. Surface roughness of the plated gold is due to the C35 etchant. Figure 5 shows the gate cross section and is indicative of the shape desired for a low resistance gate structure.

Visually, these devices are the best that have been produced on this program using the thick gate process. Electrically, improvements still need to be made. Figure 6 is a photograph of the I-V characteristics of a 0.5 x 150 micron device in quadrant four. The transconductance is approximately one-fourth the value expected for a device of these dimensions. Drain to source current modulation is not symmetrical with respect to the two source regions. One source region makes only a 20% change in drain to source current and transconductance. Several devices show this tendency, and it is the same source region on each device. Additional testing is needed to explain this observation.

Heat treatment has had a dramatic effect on lifted gate devices prepared on the program. Typically, the saturated current and transconductance would increase with heat treatment. On quadrant four plated gate devices, very little change in the I-V characteristics was observed as a result of heat treatment up to 450°C.

Although the plated gate step in the process is not optimized, definite progress has been made. Calibration of the sputtered W/Ti and gold thickness indicated that thicker films than desirable were being deposited. The deposition schedule has been changed to deposit 1000 Å W/Ti films and 500 Å thick gold



21,000X

Figure 5. Gate Cross Section

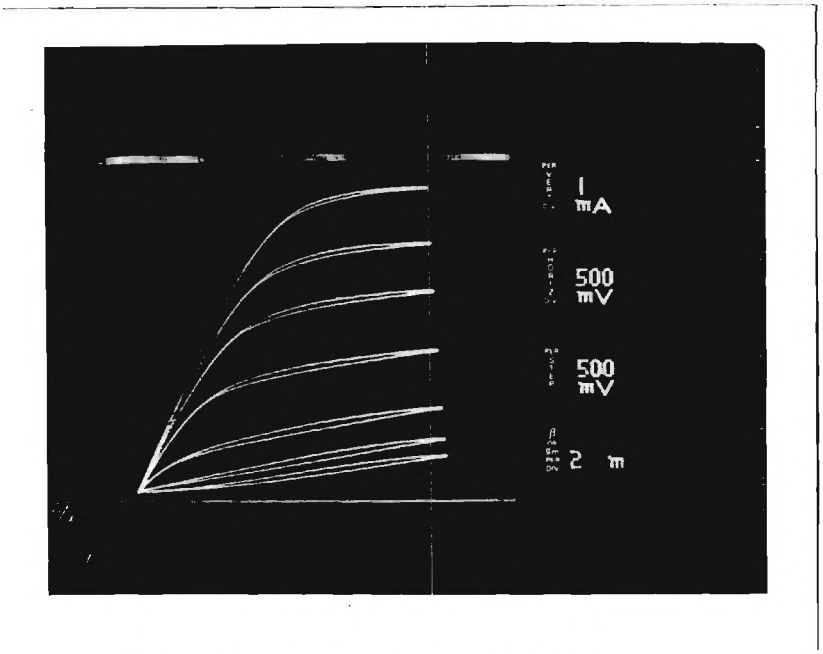


Figure 6. I-V Characteristics.

films. These thinner films will facilitate excess metal removal. Proper photoresist line widths are vital to the successful removal of the excess metal. Enlarged lines make it difficult to get the etchant in contact with the areas to be etched. In order to obtain sharp photoresist lines, the wafer surface must be free of anomalies. The ohmic contact step has been modified to improve the wafer surface.

Contract Item 7 - Ohmic Contact Process

Ohmic contact metal is deposited prior to the patterning of the narrow gate lines. Appreciable surface roughness can be caused by the alloyed ohmic metallization if the metal thickness and alloy time/temperature are not optimized. The standard Georgia Tech ohmic contact process utilizes AuGe/Ni/Au having thicknesses of 1000 Å/300 Å/1000 Å respectively. Alloying is accomplished by quickly ramping the wafer to 450°C for 30 seconds. A structure having relatively large grain size was obtained, and the surface roughness was on the order of 0.2 microns. This degree of roughness is acceptable for many processes; however, for submicron gate GaAs FETs, this roughness adds to the difficulty in delineating the gate lines.

Avantek Inc. has reported a AuGe/Ni/Au contact which has excellent surface morphology.[9] This contact is composed of AuGe/Ni/Au in thicknesses of 500 Å/50 Å/700 Å and is alloyed at 400°C.[10] Using the existing ohmic evaporation system, runs were made to determine the amount of material necessary to obtain similar thicknesses. With a source to substrate spacing of four

inches, the following weights of material, evaporated to completion, were necessary to obtain the desired thicknesses:

AuGe - 22 mg

Ni - 3 mg

Au - 30 mg.

Various alloy temperatures in the range of 360°C to 450°C were evaluated. Differences in alloy furnaces and the thermal masses involved make it difficult to state the exact alloy conditions; however, a temperature controller setting of 425°C and a dwell time of 30 seconds on the heated platen produced the best results as determined by visual inspection. Surface roughness was less than 100 A. Contact resistance tests have not been made on this new ohmic process to date, but it is expected that the contact resistance will be less than 1×10^{-6} ohm-cm^2.

PLANS FOR NEXT MONTH

- Complete thick gate process
- Continue Device Fabrication
- Deliver Additional Devices

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FINAL REPORT
PROJECT A-3459

LOW NOISE GaAs FET
PHASE–II

By

H. M. Harris
Electromagnetics Laboratory

Prepared for

SPACE AND COMMUNICATIONS GROUP
HUGHES AIRCRAFT COMPANY
EL SEGUNDO, CALIFORNIA

Under

P.O. No. S8–879406–LPY

24 July 1984

GEORGIA INSTITUTE OF TECHNOLOGY
A Unit of the University System of Georgia
Engineering Experiment Station
Atlanta, Georgia 30332

GTEES

1984

LOW NOISE GaAs FET - PHASE II

Contract period covered
3 January 1983 through 9 March 1984
P.O. S8-879406-LPY

Submitted to
Hughes Aircraft Company
El Segundo, California 90234

by

Physical Sciences Division
Electromagnetics Laboratory
Engineering Experiment Station
Georgia Institute of Technology
Atlanta, Georgia 30332

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1.0 INTRODUCTION

Gallium arsenide field effect transistors (GaAs FETs) have become the primary active components for X and Ku band low noise amplifier designs. In addition, monolithic analog microwave integrated circuits based on GaAs FET technology are becoming viable candidates for space and communications applications. Funded by Hughes Aircraft Space and Communications Group under P.O. number S8-879406-LPY, the Physical Sciences Division of the Georgia Tech Engineering Experiment Station has developed a monolithic compatible, high performance, low noise GaAs FET process. This research effort has involved the design and fabrication of a multi-layer mask set, specification and procurement of GaAs epitaxial material, submicron photolithography, Schottky barrier gate process development and the development of low loss crossover interconnections.

Results of this research effort covering the period 3 January 1983 through 9 March 1984 are presented in this report. Significant accomplishments during this effort include:

- o thick gate metallization process
- o air-bridge crossover process and
- o fabrication of submicron gate length FETs having unity gain frequencies in excess of 20 GHz.

The following sections provide specific details of design, materials and processing features leading to these results.

2.0 TECHNICAL APPROACH

Development of a low noise GaAs FET process was begun during phase I, and many processing details were resolved. Phase II was initiated to "fine tune" the processes developed during the first phase. The mask set employed in phase I was furnished by Hughes. This mask set (RFIC) is well suited for providing a variety of microwave circuit elements (filters, amplifiers and couplers) using a mature fabrication process. However, for process development and FET evaluation, a mask set having more discrete devices per unit area is desirable.

The technical approach for this effort was to design a new mask set which would provide high performance devices and at the same time facilitate process development.

Schottky barrier gates, fabricated with the proven Ti-Pt-Au electron beam evaporation process, were planned for this effort.[1] However, a different approach, using Ti/W-Au, was found to be better suited to process requirements.

3.0 MASK SET DESIGN AND FABRICATION

3.1 Design Considerations

As a result of discussions with Hughes personnel and a review of current GaAs FET literature, several design related features necessary for state-of-the-art devices were recognized. The most critical area of GaAs FET design is the Schottky barrier gate. If material quality and low contact resistances are maintained, gate length is the main factor in determining noise performance.

Gate resistance is another factor which must be considered in order to obtain good low noise devices. The use of multiple gate feeds is the primary design feature to reduce gate resistance. Multiple feeds necessitate the use of crossovers to connect the source or gate elements or multiple bond wires. Designs utilizing multiple bond wires normally have a gate structure in which the source wraps around two or more gate pads.[2] Dielectric isolation and air-bridge technology are two methods of providing crossovers. Since air-bridge technology has been used successfully for this purpose and is also well suited for inductor designs in monolithic circuits, this method was selected to provide the necessary interconnections.[3,4]

Preliminary mask set design was based primarily on the RFIC mask design and its associated design rules. Changes to the initial design were made as a result of sponsor inputs and reviews of technical reports.[4,5]

After considering processing capabilities, the following seven level mask set was proposed:

Level#	Description
1	Ohmic Contact
2	Mesa
3	Wide Gate
4	Narrow Gate
5	Plated Gate
6	Vias
7	Air-Bridge

Design rules were formulated for bridged and unbridged devices and are shown in Tables 1 and 2.

3.2 Design Implementation

Computer aided mask set design was performed on the Georgia Tech Microelectronic Research Center's Calma system. After several iterations, the design shown in figure 1 was finalized. This array contains 63 discrete FETs having gate lengths of 0.25, 0.50, 0.75 and 1.0 microns and gate widths of 75, 150 and 300 microns. A drain to source spacing of 3.5 microns is employed on all devices, and the gate to source spacing is 1.0 micron. Overall size of the array is 156 by 147 mils. Figure 2 is a plot of a discrete FET having a gate length of 0.25 microns and a gate width of 75 microns. Relationships of the various mask levels and design complexity can be seen in the plot.

A centrally located diagnostic pattern is also included

UNBRIDGED DEVICES

APPLICATION	DIMENSIONS (microns)	LEVEL TO LEVEL
gate widths	75, 150, 300	mesa to mesa
mesa length	23.5	mesa to mesa
mesa segment separation	10.0	mesa to mesa
drain to source spacing	3.5	ohmic to ohmic
gate to source spacing	1.0	ohmic to narrow gate
gate runoff of mesa	2.0	narrow gate to mesa
gate feed lines	4.0	narrow gate to narrow gate
narrow gate metal withdrawn 2.0 microns from ohmic edges nearest gate region	2.0	narrow gate to ohmic
narrow gate metal withdrawn 1.0 microns from ohmic metal elsewhere	1.0	narrow gate to ohmic
plated gate metal coincident with narrow gate metal on ohmics,	0	plated gate to narrow gate
one (1) micron wider on each side of gate feed,	1	plated gated to narrow gate
withdraw one micron on pads	1	plated gate to narrow gate
via opening withdrawn 2.0 microns from edge of plated gate level on pads	2	via to plated gate
air bridge metal coincident with plated gate level	0	air bridge to plated gate
bond pad area > 2 x 2 of free bonding area	2x2 mils	

Specific Dimensions

Gate Length (microns)	Wide Gate (microns)	Plated Gate (microns)
.25	.75	1.0
.50	1.0	1.5
.75	1.25	2.0
1.0	1.5	2.0

Table 1. Unbridged Device Dimensions

BRIDGED DEVICES

APPLICATION	DIMENSIONS (Microns)	LEVEL TO LEVEL
gate widths	75, 150, 300	-
mesa length	15.5	mesa to mesa
drain to source spacing	3.5	ohmic to ohmic
gate to source spacing	1.0	ohmic to narrow gate
gate runoff of mesa	2.0	narrow gate to mesa
narrow gate metal withdrawn 2.0 microns from ohmic edges nearest gate region	2.0	narrow gate to ohmic
narrow gate metal withdrawn 1 micron elsewhere	1.0	narrow gate to ohmic
plated gate metal coincident with narrow gate metal on ohmic	0	plated gate to narrow gate
plated gate metal withdrawn 1 micron on pads	1.0	plated gate to narrow gate
via opening withdrawn 2.0 microns from edge of plated gate level	2.0	via to plated gate
air bridge plate coincident with plated gate level on pads	0	air bridge to plated gate
bond pad area > 2 x 2 mils of free bonding area	2 x 2 mils	-

Specific Dimensions
(microns)

Gate Width / Length	Mesa Split Width	Gate Feed Width	Wide Gate Length	Plate Gate Length	Air Bridge Length	Via	Source Interconnect
.25	6	3	.75	1.0	10	6 dia.	8
.50	6	3	1.00	1.5	10	6	8
75 .75	6	3	1.25	2.0	10	6	8
1.00	6	3	1.50	2.0	10	6	8
.25	10	5	.75	1.0	15	6x11	10
.50	10	5	1.00	1.5	15	6x11	10
150 .75	10	5	1.25	2.0	15	6x11	10
1.00	10	5	1.50	2.0	15	6x11	10
.25	10	5	0.75	1.0	20	6x16	12
300 .50	10	5	1.00	1.5	20	6x16	12
.75	10	5	1.25	2.0	20	6x16	12
1.00	10	5	1.50	2.0	20	6x16	12

Table 2. Bridge Device Dimensions

within the array and contains the following test patterns.[6]

Test Pattern	Pads
Active layer CV	8, 9
Isolation test	6, 7
Greek cross for mobility measurement	5, 6, 9, 14
1 micron gate length FET	9, 10, 11
Ohmic contact test pattern	1, 2, 3, 4, 5
Gate resistance pattern	14, 15
Fat FET[7]	11, 12, 13

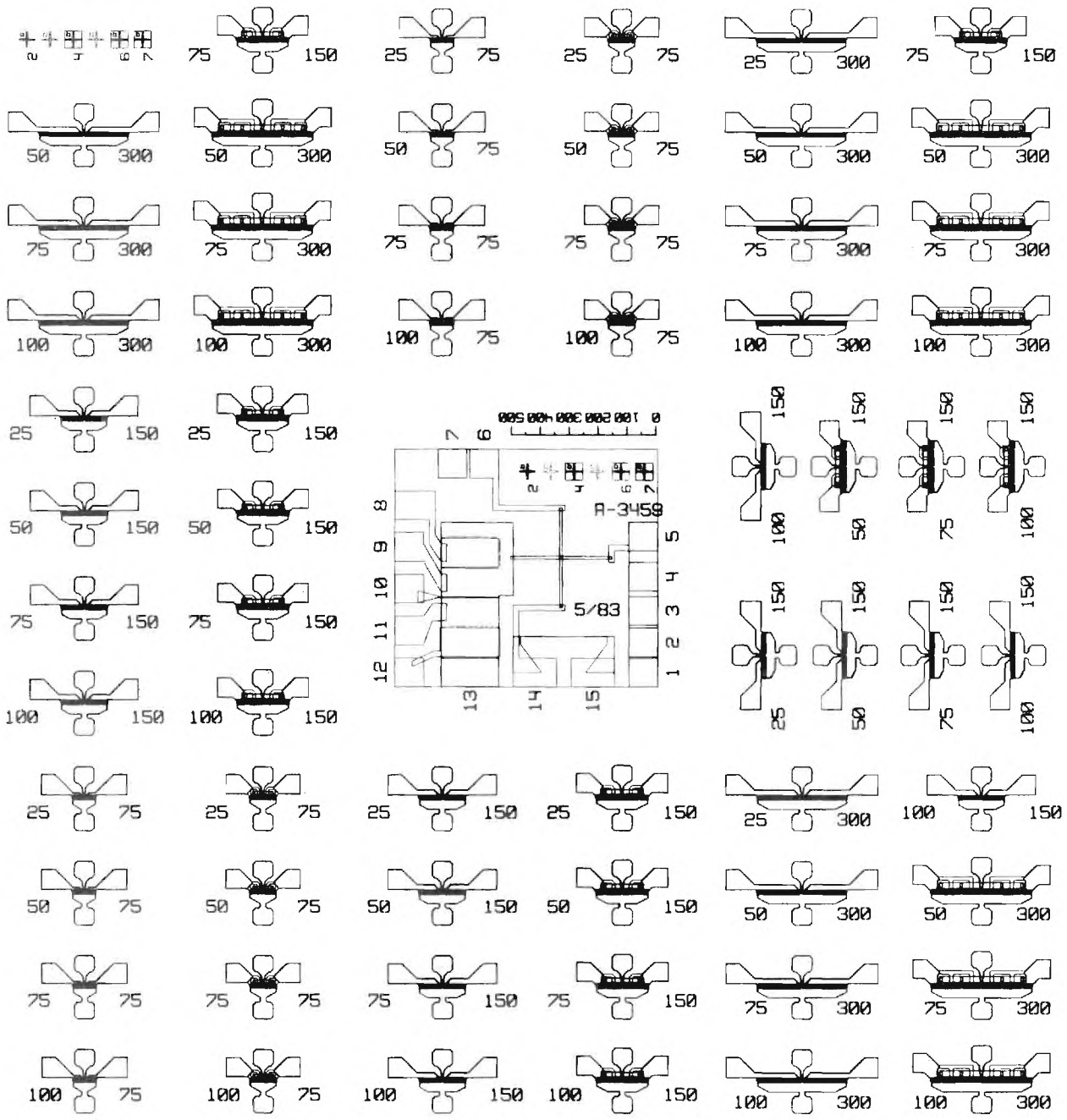


Figure 1. GaAs FET Array

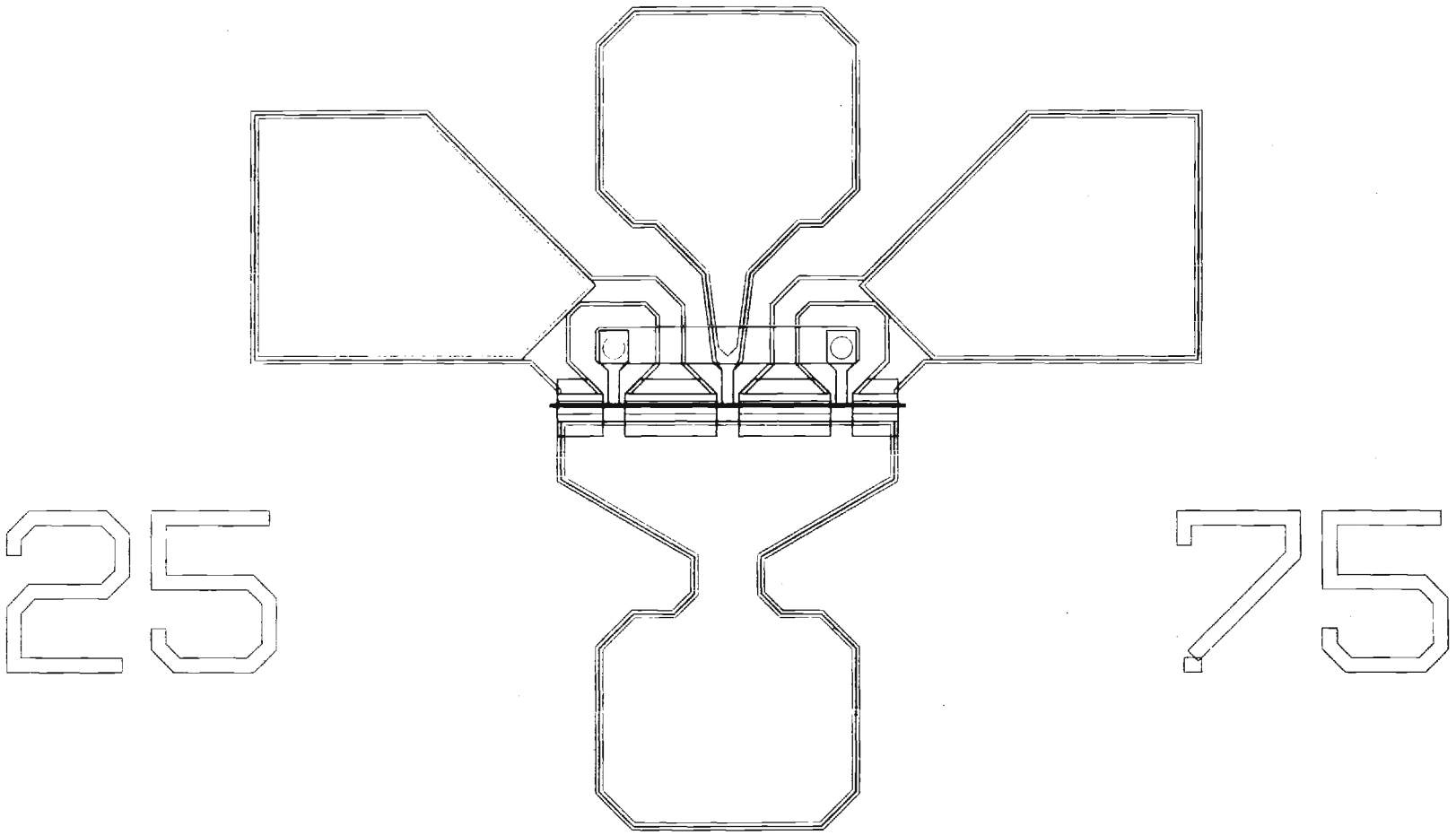


Figure 2. Discrete GaAs FET

3.3 Mask Fabrication

Mask fabrication was performed by Micro Mask Inc. using a data base tape generated on the Georgia Tech Calma System. Text was integrated into the design using an input tape from Micro Mask. Since submicron geometries were required, direct writing of the pattern onto the mask using electron beam (E-beam) mask making equipment was specified. Current E-beam equipment is limited to a minimum spot size of 0.25 microns and a guaranteed minimum line width of 0.75 + .25 microns. Micro Mask agreed to process this mask set on a best effort basis since the 0.25 and 0.50 micron geometries were below their guaranteed limits.

Data base information was converted to E-beam format and plots, generated from the E-beam formatted data, were made to check for design or translation errors. After approval of the plots, 4" by 4" chrome masks were fabricated by Micro Mask on LEU 2 micron glass plates.

3.4 Critical Dimension Verification

Only the narrow gate mask has dimensions which are smaller than the manufacturer's guaranteed minimum feature size. Optical inspection of this mask disclosed that the 0.25 micron gate lines were not clear. Precise measurement of the other gate lengths was not possible with available optical instruments. SEM was used to determine the dimensions of the 0.5 and 0.75 micron lines. Carbon coating of the mask was necessary to minimize charging. Figure 3 shows the line width of a 0.5 micron gate. Measurements of the SEM micrograph indicate that the designed 0.5 micron lines are

closer to 0.6 microns. Three-quarter micron lines were typically 0.85 microns. These dimensions are well within Micro Mask tolerances; however, they are larger than desired and lines delineated in photoresist tend to be even larger.

Alignment run-out was evaluated by patterning 1.5 inch diameter silicon wafers using the ohmic and narrow gate masks. No appreciable run-out was observed.

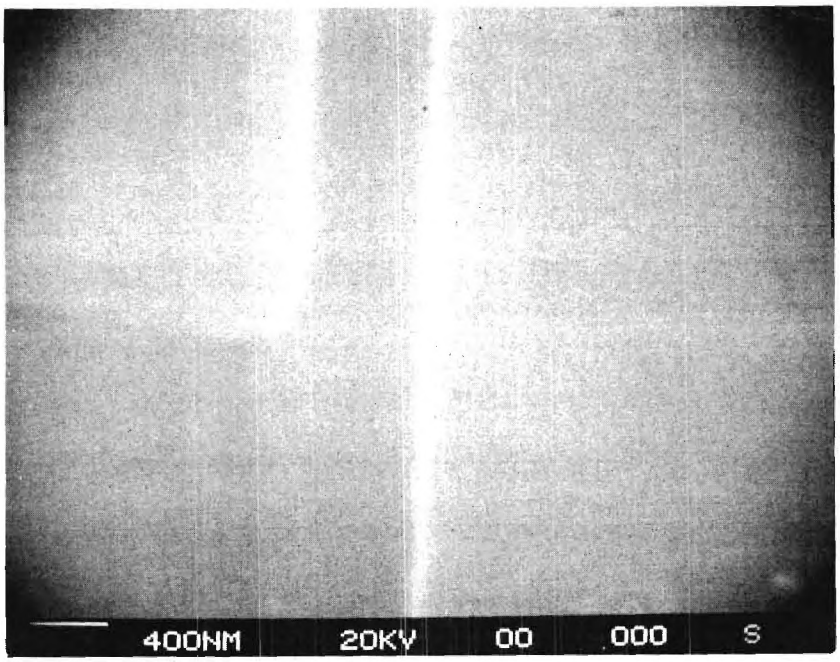


Figure 3. Micrograph of Half Micron Mask Feature.

4.0 GaAs MATERIALS

4.1 Requirements

Frequency limitations of GaAs FETs are dependent on device geometry and material parameters. These material parameters include doping concentration, doping profile, active layer thickness and quality. High purity buffer layers, with low free carrier concentration, are also extremely important.

Active layer thickness and concentration requirements are dependent on the desired pinch off voltage, saturated drain to source current and Schottky barrier formation. Since the transconductance of a FET increases with the mobility concentration product, which increases with higher concentration, gain optimization implies the use of as high a concentration as possible. However, a high concentration results in lower breakdown, higher pinch off voltage and higher saturation current for a given active layer thickness.

For the Schottky gate to have adequate control of the current transport across the channel, the gate length must be larger than the active channel depth. Typically this aspect ratio is maintained at 3:1.[8] Based on these considerations the following materials requirements were specified:

Substrate

2" diameter horizontal Bridgeman

Semi-insulating

Buffer

concentration < 5×10^{14} cm^{-3}

thickness > 2.5 microns

Active Layer

concentration = 1.8 to $3.0 \times 10^{17} cm^{-3}$

thickness = $0.15 \begin{matrix} + 0.05 \\ - 0.00 \end{matrix}$ microns

Other material requirements of material for this program which were difficult to specify or control were surface morphology and an abrupt transition from buffer to active layer. Minimal surface defects are necessary in order to obtain proper mask to wafer contact. This becomes increasingly important as gate lengths are decreased. An abrupt active/buffer layer transition results in higher device transconductance and improved pinch off characteristics.

4.2 Procurement

Georgia Tech has molecular beam epitaxy equipment and has grown GaAs active layers for FET fabrication. Devices fabricated on MBE material, using a 3 micron gate length mask set, exhibited excellent staturated current characteristics. Transconductances were on the order of 120 mS/mm. Presently the substrate size of Georgia Tech MBE material is limited to approximately 2 centimeters on a side due to the substrate holder and the source

to substrate spacing. Substrate rotation is not available and as a result, the carrier concentration across the wafer is not uniform. Epitaxial layers made with this system are well suited for many research efforts; however, for this research, larger wafers, having uniform carrier concentration across the wafer, are more suitable. As a result, a commercial supplier was utilized.

Raytheon Research Labs supplied the material for the phase I effort; however, when contacted concerning material for this work, they referred us to Raytheon Special Microwave Device Operations (SMDO). SMDO supplied three wafers having the parameters listed in table 3. Concentration profiles of these wafers are shown in figures 4, 5 and 6 respectively.

The profiles shown in these figures were obtained using a Miller capacitance technique utilizing a mercury probe for the Schottky contact. At concentrations approaching the buffer layer concentration, the accuracy is reduced, and it becomes difficult to ascertain the true characteristics of the active to buffer layer transition.

Secondary Ion Mass Spectroscopy (SIMS) is an alternate means of determining carrier concentration. Samples from these wafers were sent for this analysis; however, the results were not available in time for this report. The Georgia Tech Microelectronics Research Center is in the process of acquiring a SIMS, and this powerful materials characterization technique will be readily available on future research.

Wafer Identification Numbers

15H10

15I35

16M36

Substrate

2" Diameter LEC

15H10 - undoped

15I35 - lightly chromium doped (0.5 ppm)

16M36 - lightly chromium doped (0.5 ppm)

Buffer layer

Free Carrier concentration < $1 \times 10^{14} cm^{-3}$

Thickness > 2.5 microns

Active Layer

Wafer No.	Concentration (cm^{-3})	Thickness (microns)
15H10	1.6×10^{17}	0.16
15I35	2.0×10^{17}	0.17
16M36	2.0×10^{17}	0.16

Table 3. GaAs Material Parameters.

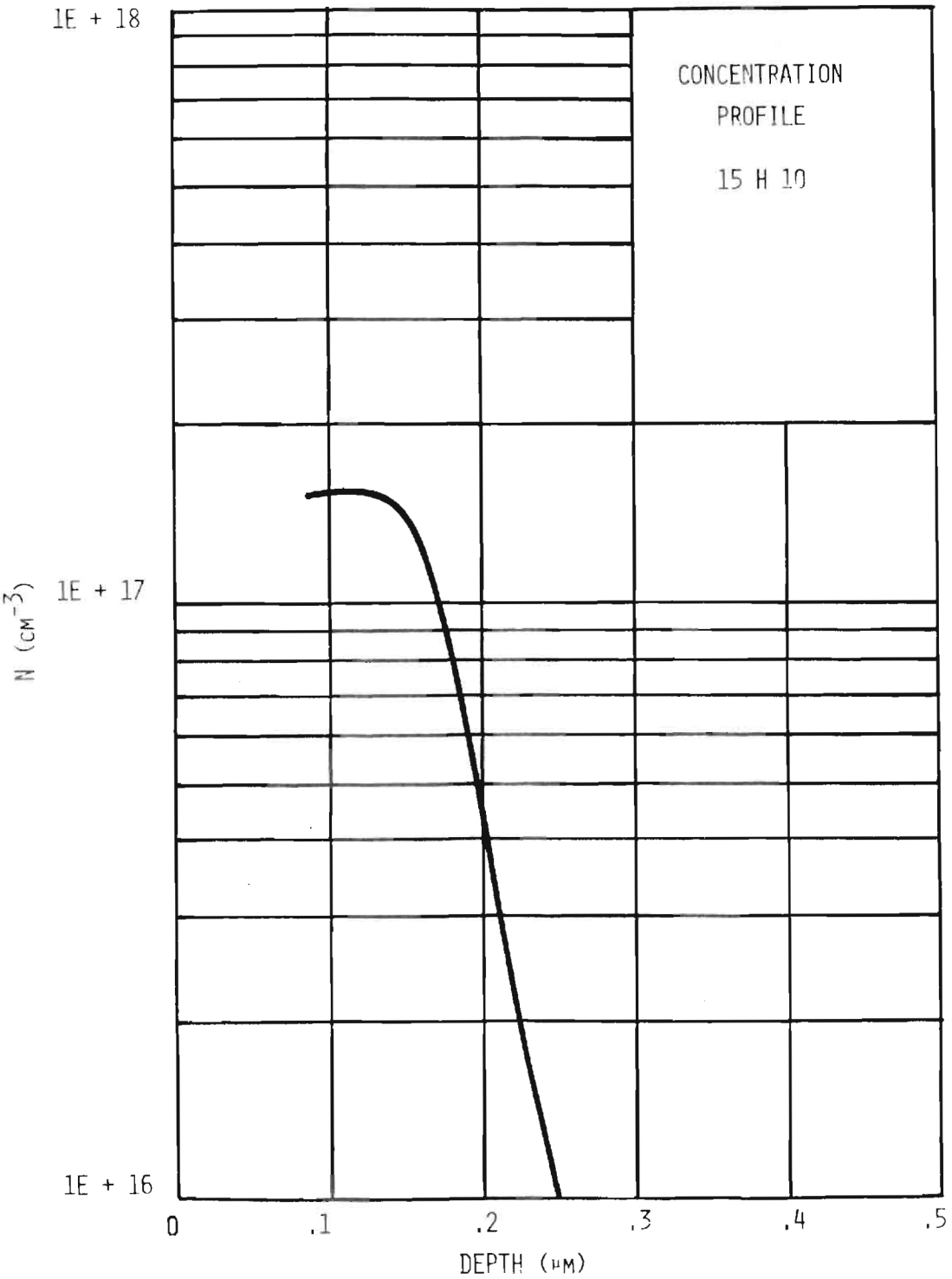


Figure 4. Concentration Profile 15H10

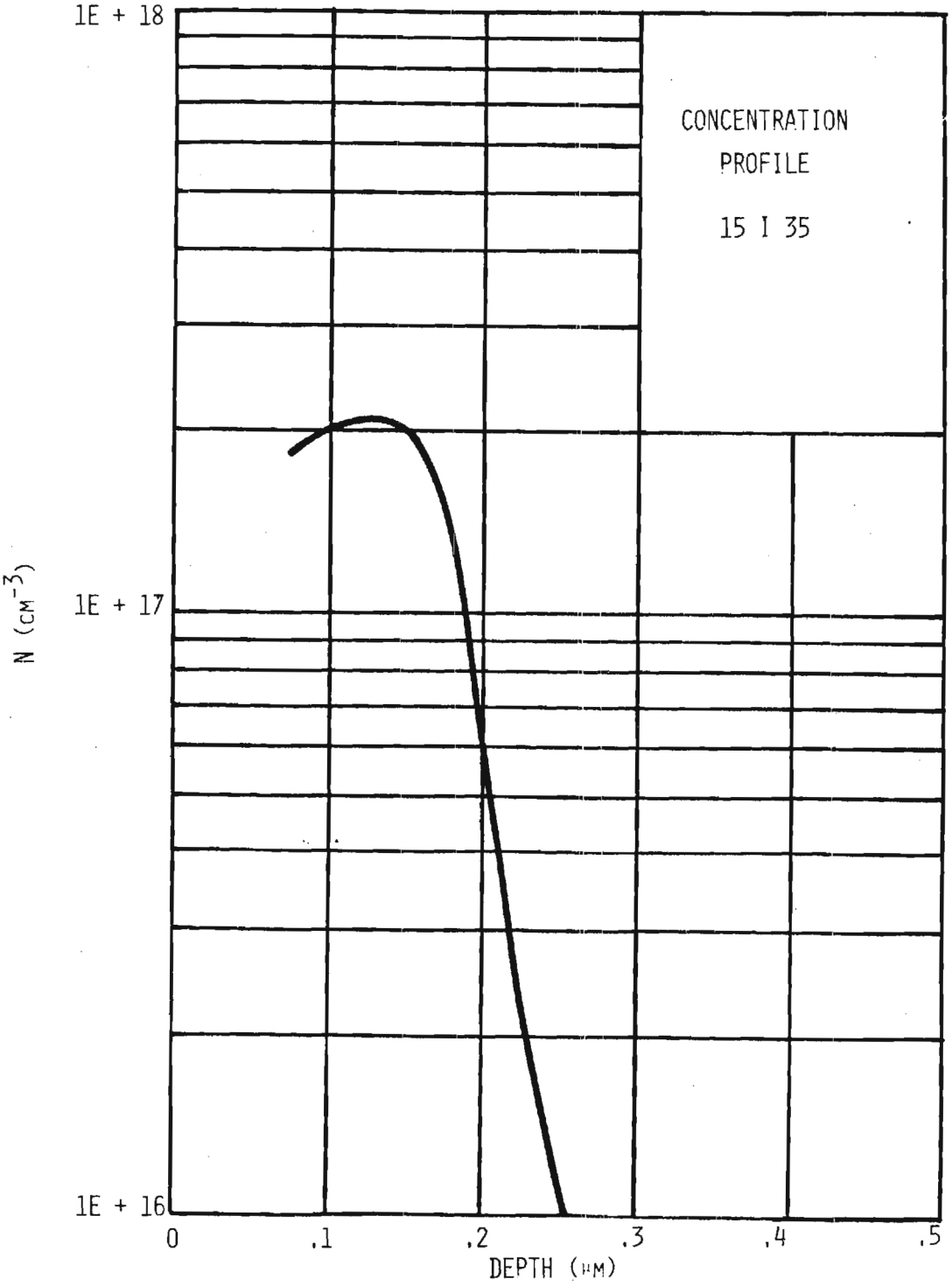


Figure 5. Concentration Profile 15I35

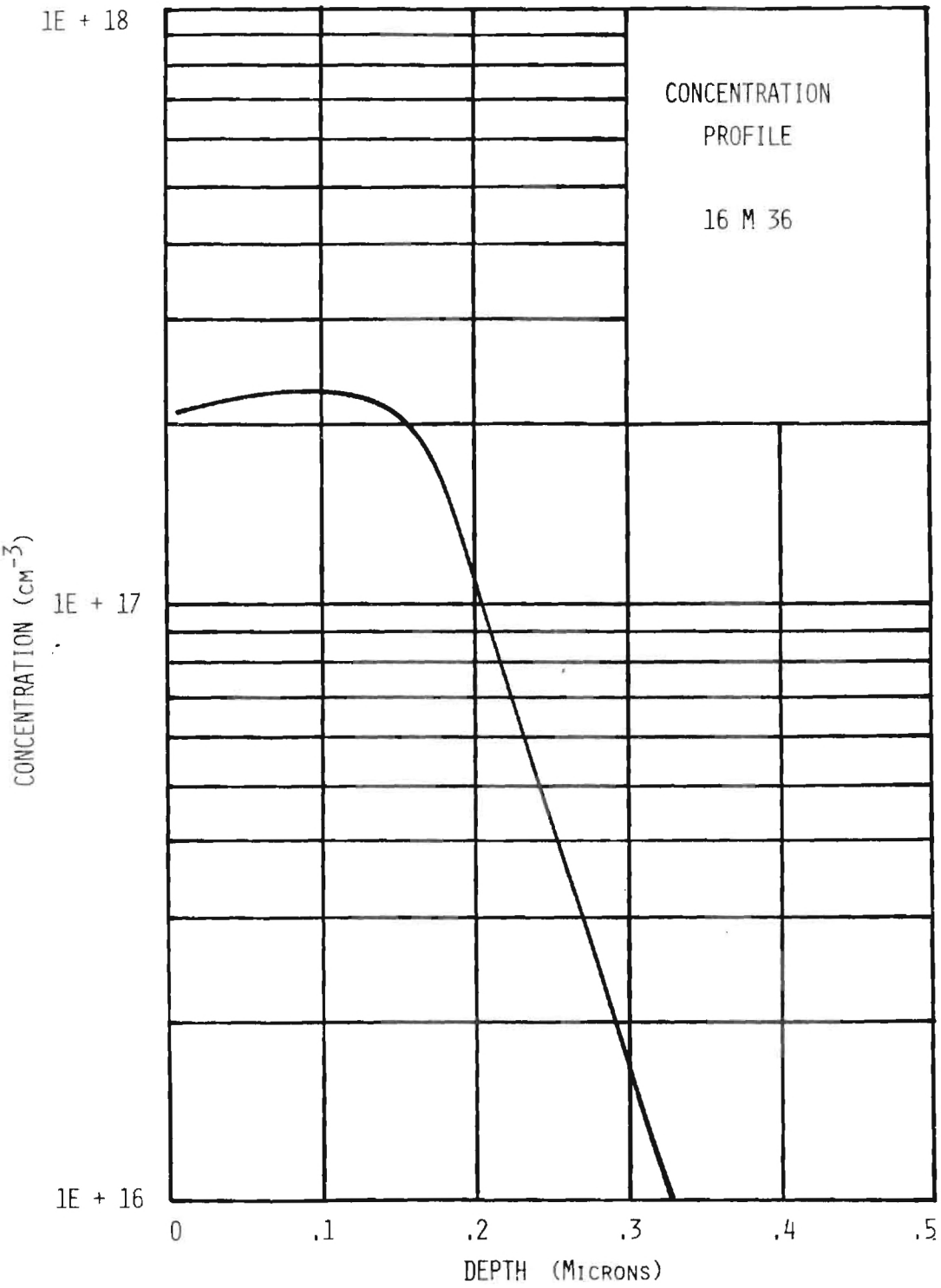


Figure 6. Concentration Profile 16M36

It should be noted that these wafers were LEC rather than the specified HB. HB substrates were not available at the time the order was placed. Other investigators have reported that HB substrates provide more consistent results than LEC material and are less prone to cracking.[9]

Near the end of this phase of work it was suggested that a retrograde concentration profile be evaluated in an attempt to improve the device transconductance under bias conditions. VPE material having a concentration spike near the buffer/active layer interface has been received, but time has not permitted device fabrication. The results reported in the following sections are on devices made from the uniformly doped active layers listed above.

5.0 PROCESS DEVELOPMENT

5.1 Background

A low noise GaAs FET fabrication process was developed during phase I and actual devices were fabricated. Phase I devices utilized a lifted gate structure and had no provisions for crossover interconnects. These two areas received major emphasis during phase II. In addition, the ohmic contact and photolithographic processes were refined.

5.2 Photolithography

Delineation of the submicron geometries is one of the most important processing steps. A Karl Suss MJB3/HP mask aligner was purchased for this research. Mid UV optics (310 nm) were installed, and the power supply was calibrated to provide a power density of 12.5 mW/cm^2. Hard contact printing was employed for each masking step.

Initially, exposure and development tests were made to establish optimum conditions (1 to 1 replication of the mask pattern to the photoresist). Shipley microposit 1350J photoresist (thinned 3 to 1) was applied to test wafers and baked at 95°C for 25 minutes prior to exposure. Photoresist thickness was 0.7 microns as measured after development. Optimum conditions are dependent on the equipment and process techniques employed. For this process at Georgia Tech, an exposure energy of 250 mJ/cm^2 and a development time of 25 seconds (Microposit 351 diluted 1 part to 3 1/2 parts H_2O) were optimum.

As each processing step was optimized, it became necessary to tailor the photoresist to the specific application. The standard process is used for the mesa photoresist pattern (with the addition of a 110°C postbake for 10 minutes to make the resist more etch resistant. Ohmic contact metal deposition is performed by evaporation, and a lift-off process is used to define the metal pattern. Photoresist is applied, baked and exposed as described above; however, before development, a chlorobenzene soak and subsequent bake are performed to provide an overhang structure for improved lift-off. Development time is then increased to 55 seconds.

Photoresist, thinned 2:1, is used for the narrow gate process. Having a thickness of 5000 angstroms when spun at 6000 rpm, this resist makes it possible to obtain linewidths near the mask dimensions. An exposure energy of 300 mJ/cm^2 and a development time of 25 seconds resulted in clear patterns.

Thicker resist is required at the plated gate step. Resist (3:1) is spun at 4000 rpm, baked as normal, exposed for 33 seconds (412 $mJ)/cm^2$), and developed 30 seconds.

Via and air-bridge photoresist processes are the same. Full strength 1350J is spun at 4000 rpm, baked as normal, exposed 3 minutes (2250 mJ/cm^2) and developed 45 seconds. These variations in the photoresist procedure result in a more complex process, but are necessary to achieve the desired results. Specific details of each photoresist step are contained in the appendix.

5.3 Ohmic Contact Process

Ohmic contact metal is deposited prior to the patterning of the narrow gate lines. Appreciable surface roughness can be caused by the alloyed ohmic metallization if the metal thickness and alloy time/temperature are not optimized. The standard Georgia Tech ohmic contact process utilizes AuGe/Ni/Au having thicknesses of 1000 Å/300 Å/1000Å respectively. Alloying is accomplished by quickly ramping the wafer to 450°C for 30 seconds. A structure having relatively large grain size is obtained, and the surface roughness is on the order of 0.2 microns. This degree of roughness is acceptable for many processes; however, for submicron gate GaAs FETs, this roughness adds to the difficulty in delineating gate lines.

Avantek Inc. has reported a AuGe/Ni/Au contact which has excellent surface morphology.[10] This contact is composed of AuGe/Ni/Au in thicknesses of 500 Å/50 Å/700 Å and is alloyed at 400°C[11]. Using the existing ohmic evaporation system, runs were made to determine the amount of material necessary to obtain similar thicknesses. With a source to substrate spacing of four inches, the following weights of material, evaporated to completion, were necessary to obtain the desired thicknesses:

AuGe - 22 mg

Ni - 3 mg

Au - 30 mg.

Various alloy temperatures in the range of 360°C to 450°C were evaluated. Differences in alloy furnaces and the thermal masses involved make it difficult to state the exact alloy conditions;

however, a temperature controller setting of 425°C and a dwell time of 30 seconds on the heated platen produced the best results as determined by visual inspection. Surface roughness was less than 100 A.

Ohmic contact resistance was evaluated using unequally spaced contact pads shown in figure 1. Resistance between adjacent pads was measured using a precision current source, digital multimeter, and probe station. Contact resistance in units of ohm-millimeters was calculated using the equation[12]

$$r_c = \frac{R_{ij}l_{jk} - R_{jk}l_{ij}}{2(l_{ij} - l_{jk})} \quad W$$

where R_{ij} and R_{jk} are the resistances between pads i and j and j and k, respectively, l_{ij} and l_{jk} are the distances separating the pads and W is the pad width in millimeters.

Measurements on several runs resulted in an average contact resistance of 0.3 ohm-mm. Although the run to run averages were reasonably consistent, pad to pad measurements varied over a wide range (0.05 to 0.8 ohm-mm). It was evident from this evaluation that small errors in the measurement of the distance between pads or extraneous resistance due to probe contacts could cause significant errors in the resultant contact resistance.

5.4 Thick Gate Process

With respect to processing simplicity, gate formation using a lift-off process is unsurpassed. However, as the gate length decreases, the gate resistance increases to unacceptably high

values unless provisions are made to modify the gate length to height aspect ratio or to permit multiple gate feeds. A plated gate process utilizing multiple gate feeds, was developed in this research to minimize the gate resistance.

Figure 7 is a cross sectional drawing of the characteristics of a lifted gate and a plated gate process. In the lifted gate process, the gate metal cross-section becomes triangular due to closure of the photoresist opening during metal deposition. As gate lengths are reduced, this triangular gate structure results in high gate resistance.

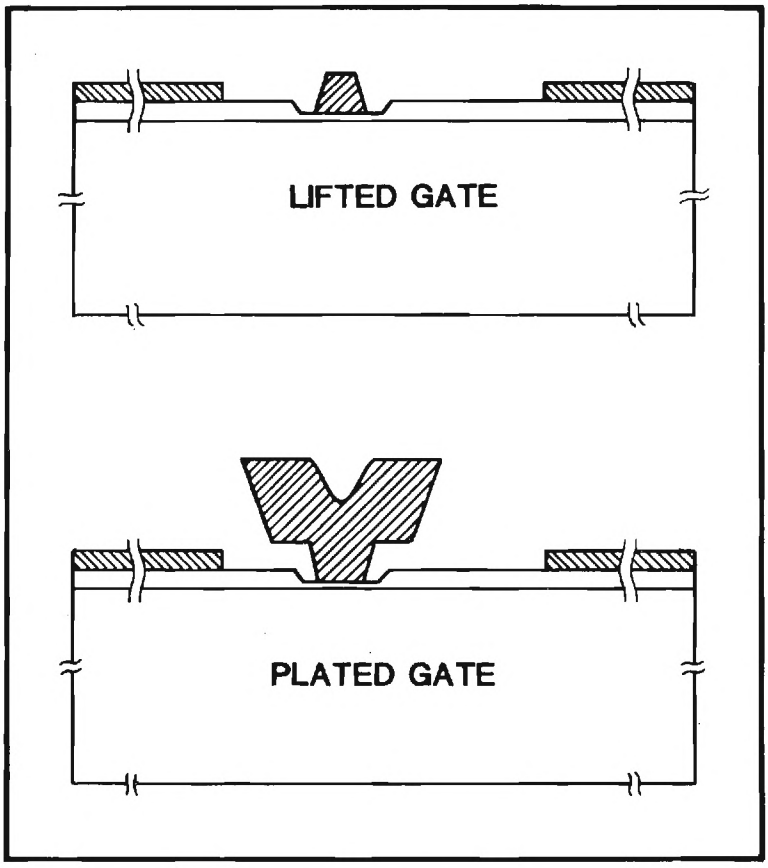


Figure 7. Gate Cross Sections

Low gate resistance is maintained in the plated gate process by the inclusion of thick plated gold on top of the narrow gate metal. This process requires an additional masking step and necessitates the use of narrow gate metals which can be easily patterned by dry or wet chemical etching.

Schottky contacts to GaAs using Ti-Pt-Au have provided excellent results on mixer diodes and FET gates patterned by a lift-off technique.[1,8] However, platinum is a difficult material to etch, and as a result, a different gate metal system was utilized.

Aluminum and titanium/tungsten (Ti/W) have been shown to exhibit stable electrical characteristics when subjected to high temperature storage tests.[13] However, aluminum is susceptible to degradation due to moisture and ionic contamination, and as a result was not considered in this effort.

Since stable characteristics have been reported on FETs utilizing Ti/W gates, a sputtering target composed of 90% W and 10% Ti was purchased. To evaluate diode characteristics, mixer diodes having Ti/W gates were fabricated and compared to mixer diodes fabricated with electron beam evaporated Ti-Pt-Au Schottky contacts. GaAs material from the same wafer (8A501) was used on both test pieces. Ti/W-Au was sputter deposited at 50 watts to minimize heating of the photoresist.

Removal of the photoresist was accomplished by the tape lift-off technique. Substrates were thinned by mechanical lapping, and a AuGe-Ni-Au ohmic contact was evaporated on the

back side of the wafer. The ohmic contact was alloyed at 450°C for 30 seconds in forming gas.

Two separate runs were made to check reproducibility. Eight diodes from the first run were electrically characterized. Ideality factors ranged from 1.13 to 1.23 and averaged 1.18. Figure 8 is a plot of the current-voltage characteristics of a typical diode. Figure 9 is a curve tracer photograph showing both forward and reverse characteristics. DC electrical performance of these diodes was comparable to the E-beam evaporated devices.

Diodes from the second run had ideality factors ranging from 1.13 to 1.16 with an average value of 1.14. Eight diodes from this run were tested. Figure 10 shows the curve tracer signatures of a typical diode. Current-voltage characteristics are plotted in Figure 11.

Mixer diodes made with Ti-Pt-Au typically had ideality factors on the order of 1.13 to 1.17. Based on this comparison and the repeatable results obtained, it was concluded that Ti/W is a suitable material for the Schottky gate contact. However, in addition to having good diode characteristics, the gate metal must be patternable.

Figure 12 is a cross section diagram of the thick gate process developed during this phase. Photoresist is patterned and the GaAs is etched in the gate region to the desired saturation current. Schottky metal is sputter deposited and the wafer is coated with another layer of resist. Patterning of the top layer of resist defines the areas which are subsequently plated with

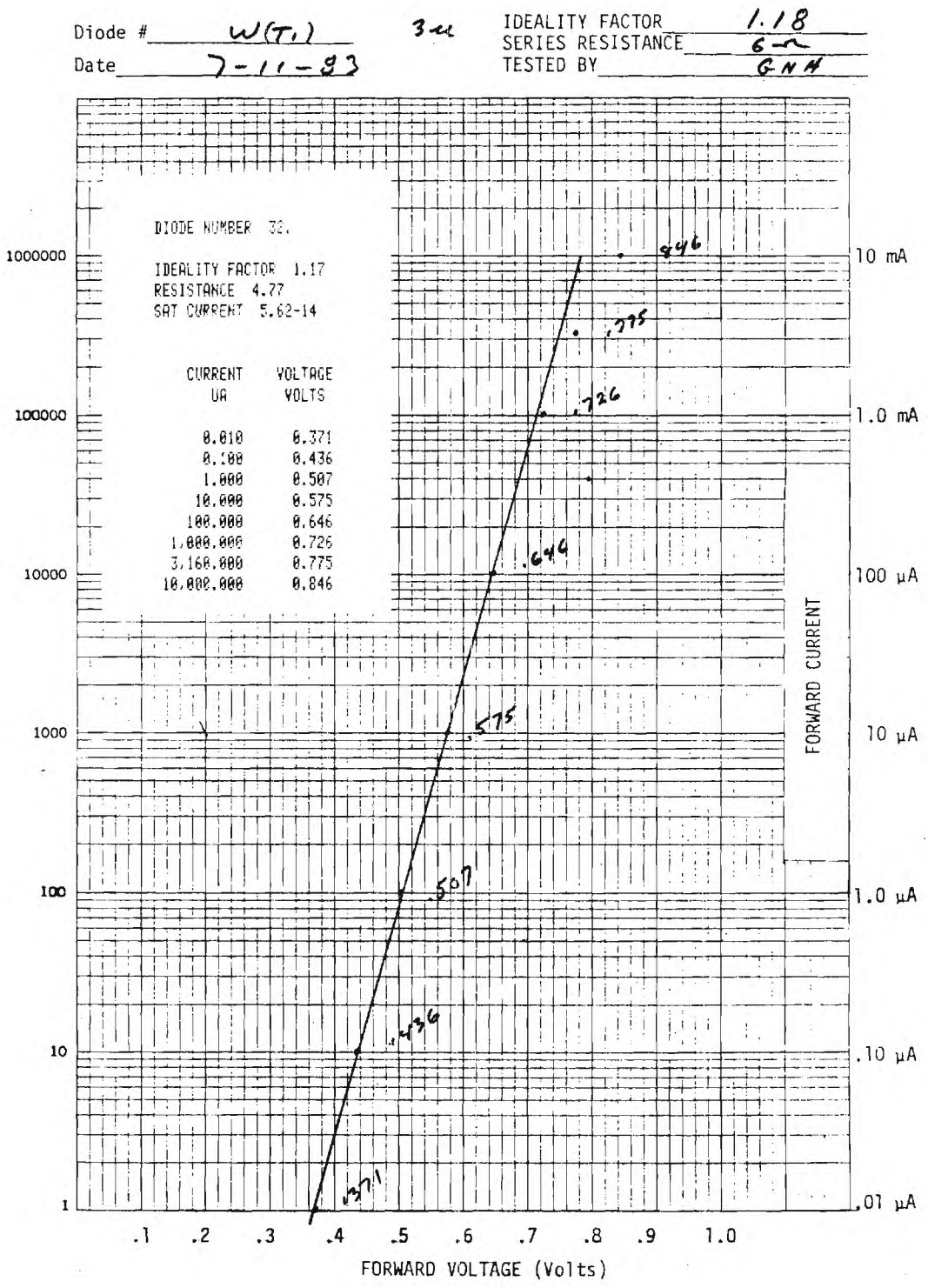


Figure 8. Mixer Diode Current-Voltage Plot First Run.

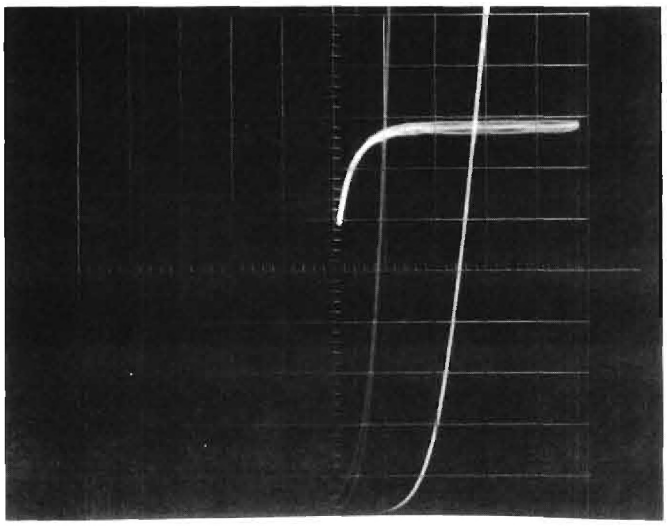


Figure 9. Curve Tracer Signatures of Mixer Diode - First Run.

Upper Traces: Horiz. 2.0V/cm
Vert. 0.1ma/cm

Lower Traces: Horiz. 0.1V/cm
Left Vert. 0.01mA/cm
Right Vert. 1.0mA/cm

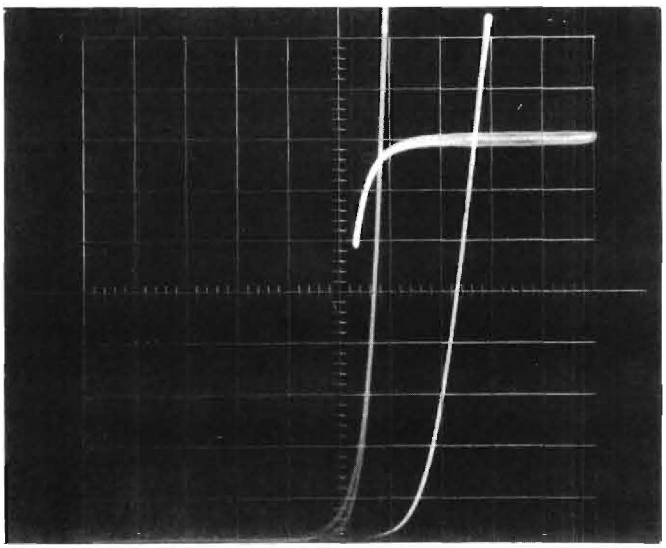


Figure 10. Curve Tracer Signatures of Mixer Diode - Second Run.

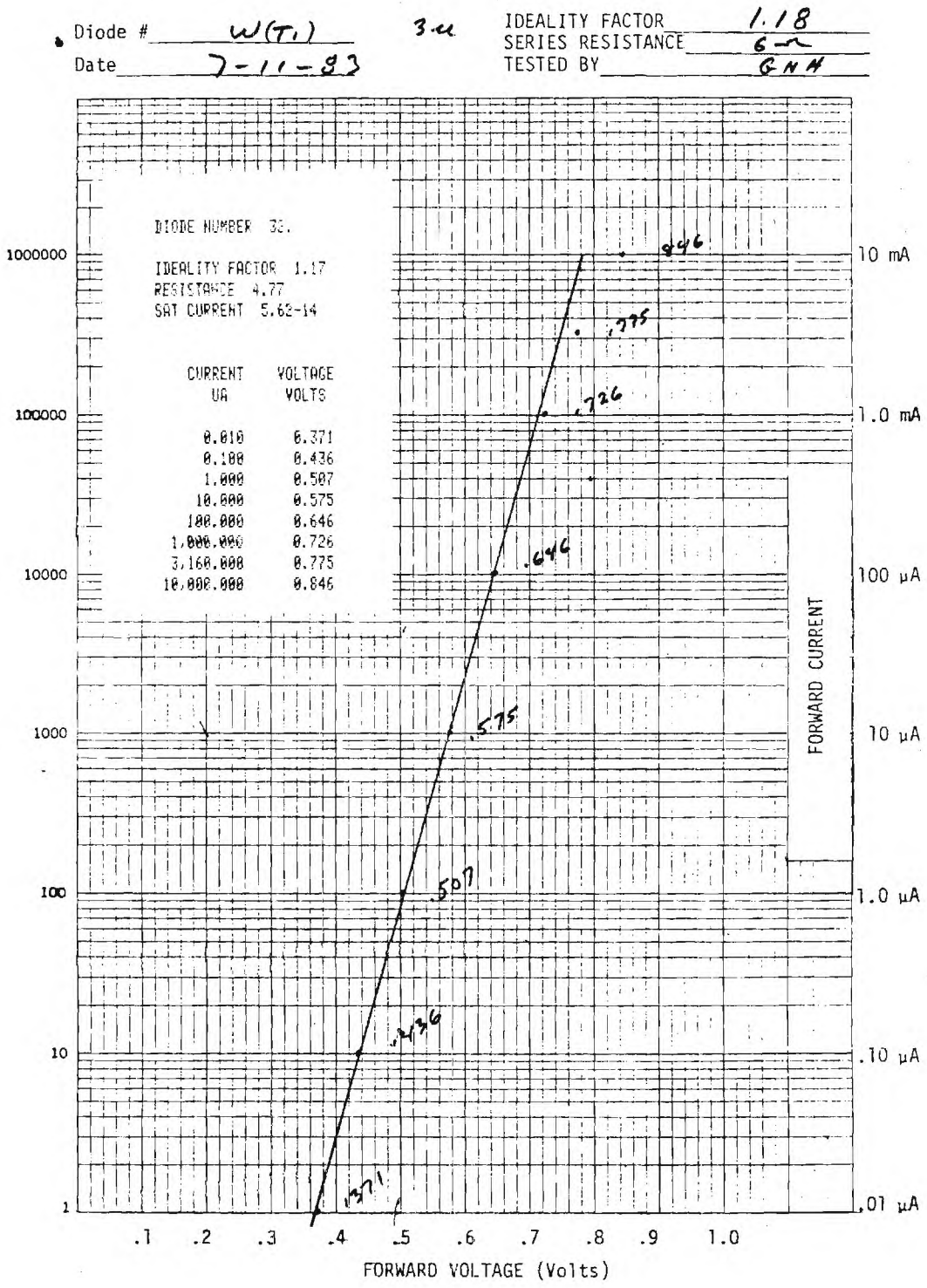
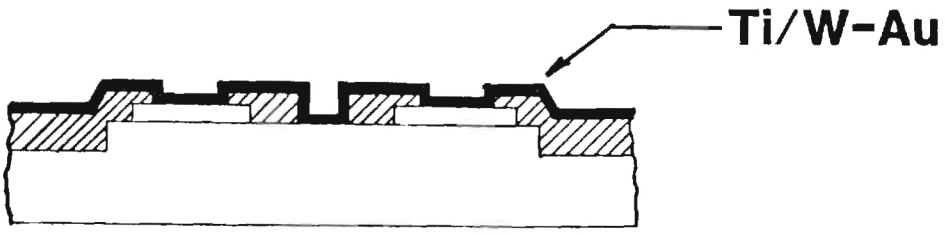
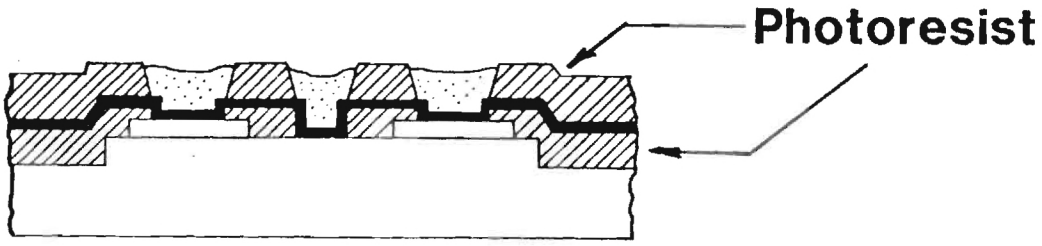


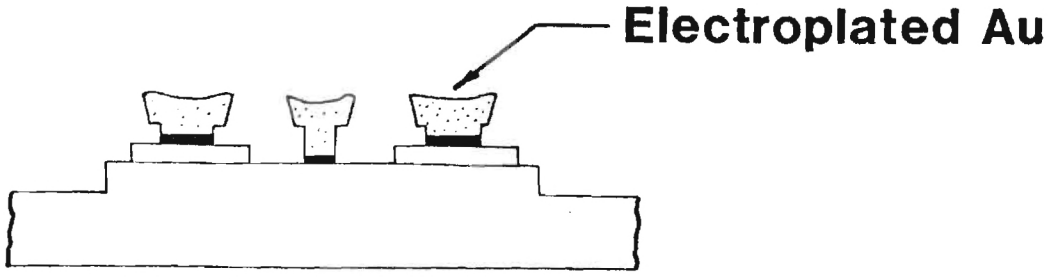
Figure 11. Mixer Diode Current-Voltage Plot Second Run.



a. Ti/W-Au Sputter Deposition over Patterned Wafer.



b. Second Level Photoresist Patterning and Selective Gold Electroplating.



c. Removal of Photoresist and Excess Ti/W-Au Metallization.

Figure 12. Thick Gate Process Cross Sections

gold. The gate structure is delineated by removing the top layer of resist, etching the underlying sputtered metallization and removing the bottom photoresist layer. This sequence of processing steps was the most difficult aspect of process development.

Various techniques were evaluated to etch Ti/W metallization. In order to properly delineate the gate metallization, these etchants must be compatible with photoresist and the underlying GaAs. Plasma etching of Ti/W with PDE-100 (a CF_4 - O_2 mixture from LFE) was first attempted. Samples, which were plasma etched immediately after they had been deposited, etched well. However, samples which were subjected to gold etch solutions or chromic acid did not etch in PDE-100. Using a light plasma strip in O_2 prior to PDE-100 improved reproducibility; however, some areas were not completely cleared.

Planar plasma etching of the Ti/W was also attempted using a Technics PEIIA system. Etching was accomplished at a power level of 10W for 10 minutes at 60°C. Results were better than those obtained with the barrel reactor; however, some nonuniform etching was still present and devices fabricated with this procedure had poor I-V characteristics.

Wet chemical etching was next evaluated. A photoresist compatible tungsten etch, described by Shankoff, was first employed.[14] No appreciable etching was noted. A component for etching titanium was required. Nine parts of tungsten etch were mixed with one part HF, and the etching experiment was repeated

with successful results. However, this solution is not chemically compatible with GaAs.

Concentrated hydrogen peroxide has been used to etch Ti/W in a VLSI silicon bipolar process.[15] H_2O_2 was first evaluated for its compatibility with GaAs and photoresist. GaAs FETs, fabricated with a lift-off process, were immersed in H_2O_2 for an extended period of time. No apparent change in I-V characteristics was observed. In addition, tests with photoresist coated wafers indicated that the positive photoresist was not affected by the H_2O_2.

Etching tests on Ti/W using concentrated H_2O_2 resulted in uniformly etched patterns. The etch rate at room temperature was on the order of 100 angstroms per minute.

Removal of the bottom layer of photoresist is the last step in the gate delineation process. Although temperature measurements indicate that the resist is not heated to excessively high temperatures, solvents such as acetone are not effective in removing the resist. By experimentation it was found that a combination of UV exposure, chemical remover, and plasma stripping could be used to completely remove the resist. UV exposure was followed by a short duration development in the standard developer. This was followed by H_2O_2 etchant to remove any residual Ti/W. Microposit 140 remover (50°C) removed almost all of the resist. The residue was successfully removed with an oxygen plasma. Several evaluation runs were made using this thick gate process which is summarized below:

- apply thin photoresist (5000 angstroms) and pattern with narrow gate mask,
- perform gate recess,
- sputter Schottky metals,
- apply thick photoresist (1 micron) and pattern with the plated gate mask,
- electroplate gold,
- expose and develop top layer of resist,
- etch the thin gold with techni-strip,
- remove the Ti/W with H_2O_2,
- dissolve the photoresist with microposit 140 for 10 minutes,
- remove any residue by plasma stripping at 350 watts for 8 minutes in oxygen.

Figures 13 and 14 are SEM micrographs of the gate region after the excess metal and photoresist were removed.

5.5 Air Bridge Process

Low gate resistance is critical in obtaining good low noise characteristics at high frequency. Multiple gate feeds reduce the gate resistance at the expense of a more complex fabrication process. Multiple gate feeds are provided in this process by interconnecting the gate feed lines with air bridges. Bridges, 10 microns long, are utilized for 75 micron wide devices. Bridges, 15 and 20 microns, are employed on 150 and 300 micron devices respectively. Minimum via contacts are 6 microns in diameter and larger where applicable. Two bridges are required for 75 to 150

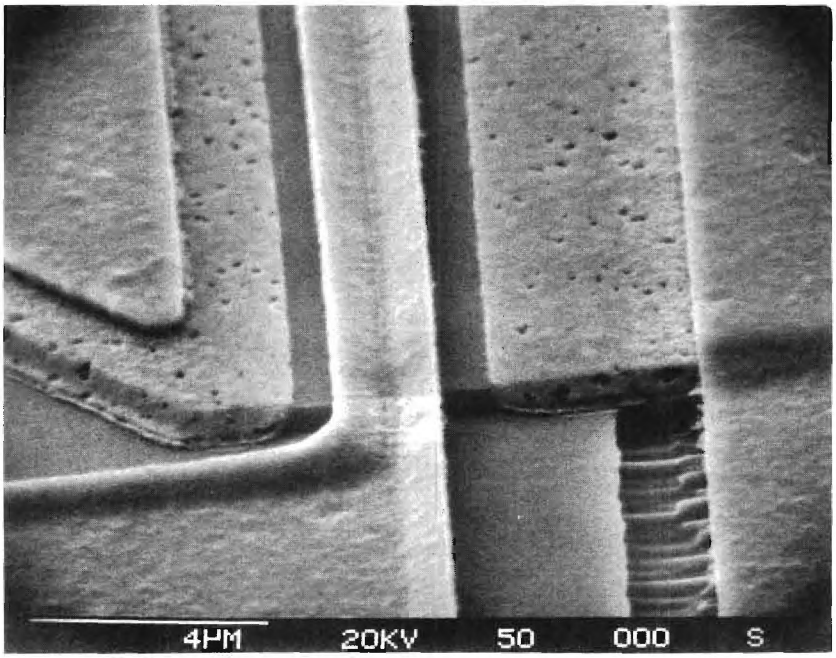


Figure 13. FET Gate Region

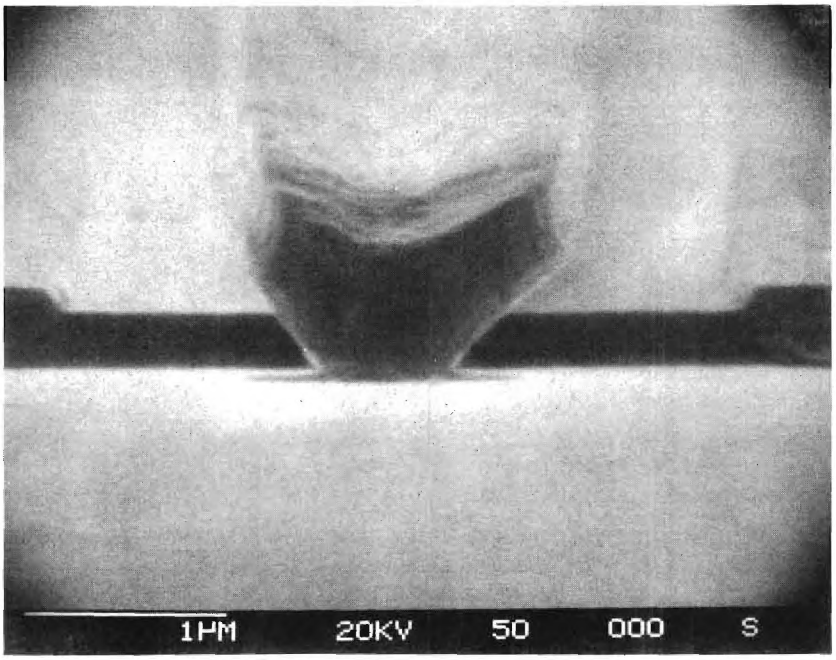


Figure 14. Gate Cross Section

micron devices having 3 gate feeds. Four bridges are utilized on the 300 micron devices.

Fabrication steps involved in this process include:

- Vias - to contact plated gate metal
- Metal Deposition - to provide a contact layer for plating
- Air Bridge Photoresist - to open areas for the air bridge metal
- Electroplate - to provide a thick metal layer which constitutes the bridge
- Photoresist Removal - to remove top resist layer
- Thin Metal Etch - to isolate the desired air bridge metal
- Photoresist Removal - to remove bottom resist layer

This process is very similar to the thick gate process in that thin metal and photoresist must be removed after electroplating the air bridge region. Gold electroplating was initially performed in the standard plating bath made up of Sel Rex Pur-A-Gold 401 solution. Grain size of the deposit was much larger than desired. Discussions with Hughes concerning this problem led to an evaluation of Sel Rex BDT 510 plating solution. Pur-A-Gold 401 is a neutral pH, cyanide based solution having a purity of deposit of 99.99+%. BDT 510 is an alkaline, noncyanide based, solution having a 99.99% purity of deposit. Solution pH is approximately 9, and a brightener is used to produce a non-crystalline structure.

Since this solution is alkaline, there was a concern that the photoresist might be damaged by the plating solution. Prior to purchase of the BDT 510 solution, a sodium hydroxide solution, having a pH of 10, was prepared, and photoresist samples were evaluated to determine the effects of basic solutions. No apparent deterioration of the photoresist was observed.

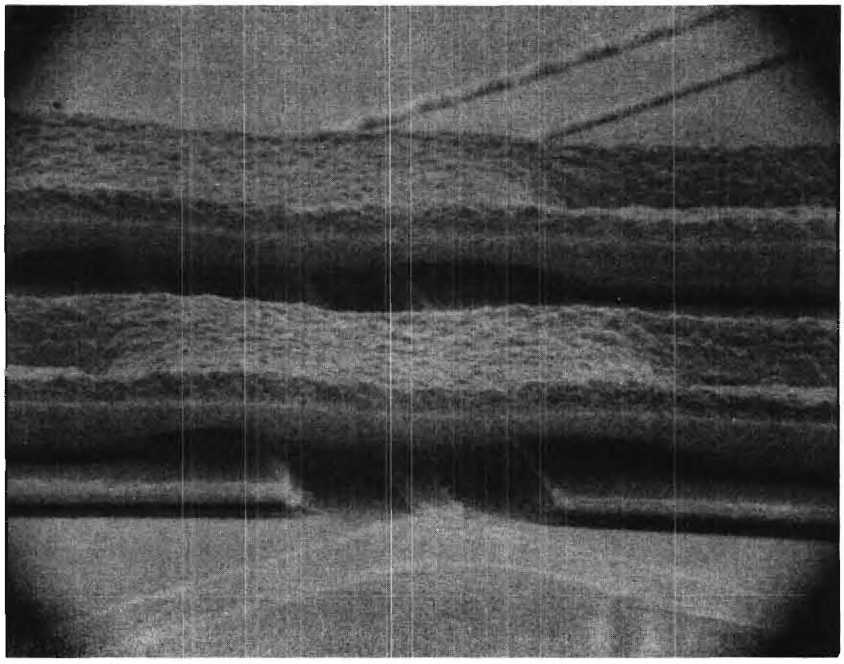
Plating tests were performed and conditions optimized to provide films with smooth surface morphology. Conditions which gave the best results were:

- Temperature = 50°C,
- Current density = 3.6 mA/cm^2,
- Vigorous agitation and
- An anode to cathode ratio > 2:1.

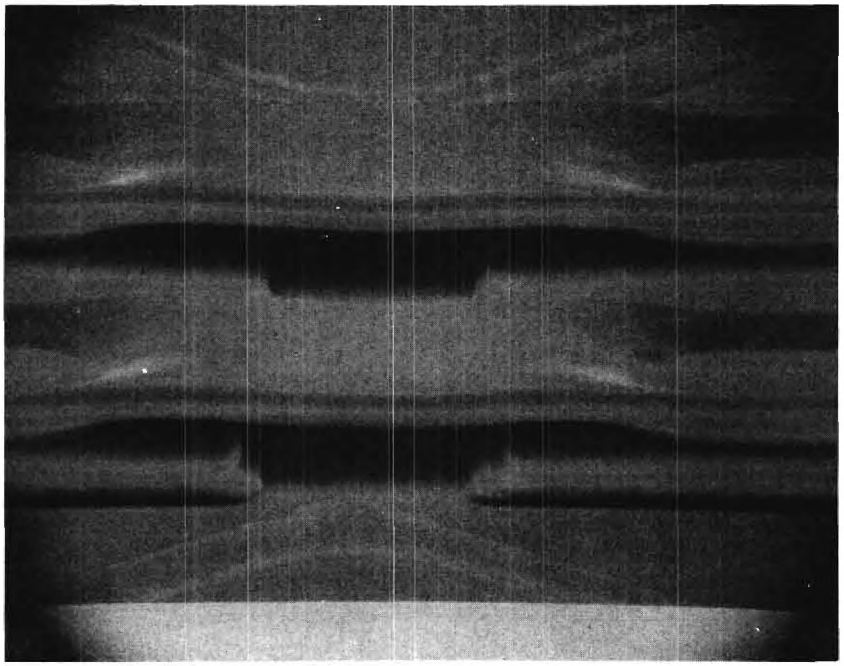
Figure 15 is a comparison of gold plating using the Pur-A-Gold 401 solution (a) and the BDT 510 solution (b). Surface morphology is much improved with the BDT 510 solution.

Gold electroplating is used for the thick gate and air bridge processes. The surface finish obtained with BDT 510 is desirable for the air bridge process and is practically a necessity for the plated gate process where near micron geometries are involved.

Delineation of the air bridge was accomplished in the same manner as the thick gate patterning. The use of thicker photoresist layers necessitated longer soak times in the remover. An oxygen plasma strip was used to remove residual photoresist.



PUR-A-GOLD-401



BDT 510

Figure 15. Comparison of Gold Plating Processes

6.0 DEVICE FABRICATION

Figure 16 is a block diagram of the general processing steps involved in this low noise GaAs FET fabrication procedure. Appendix A is a process check-list containing all the fabrication steps. Appendix B contains detailed process instructions.

A summary of the wafer processing is shown in table 4. Most of these runs were processed during process development and as a result are not representative of a mature fabrication process.

Run No.	Comments
15H10-1 -	Terminated when isolation pads came off during mesa etch
15H10-2 -	Used for ohmic contact test
15H10-3 -	Processed through thick gate step, could not remove excess metal and underlying resist
15H10-4 -	Could not remove excess metal and resist
15H10-5 -	Lifted gate process, working devices were fabricated
15H10-6 -	Wafer piece not used due to shape and size

15H10-7 - Lifted gate process low g_m, low I_{dss}

15I35-1 - Terminated when isolation pads came off

15I35-2 - Processed with alternate thick gate process, 0.5 and 0.75 micron devices not properly defined, working 1.0 micron devices were obtained.

15I35-3 - Oxide assisted process, working devices fabricated, g_m and I_{dss} low

15I35-4 - Oxide assisted process, low g_m, high R_{ds}

15I35-5 - First thick gate run to be processed through all steps. Reasonable g_m, I_{dss} and yield

15I35-6 - Thick gate run similar to 15I35-5, better yield

Table 4. Wafer Processing Summary

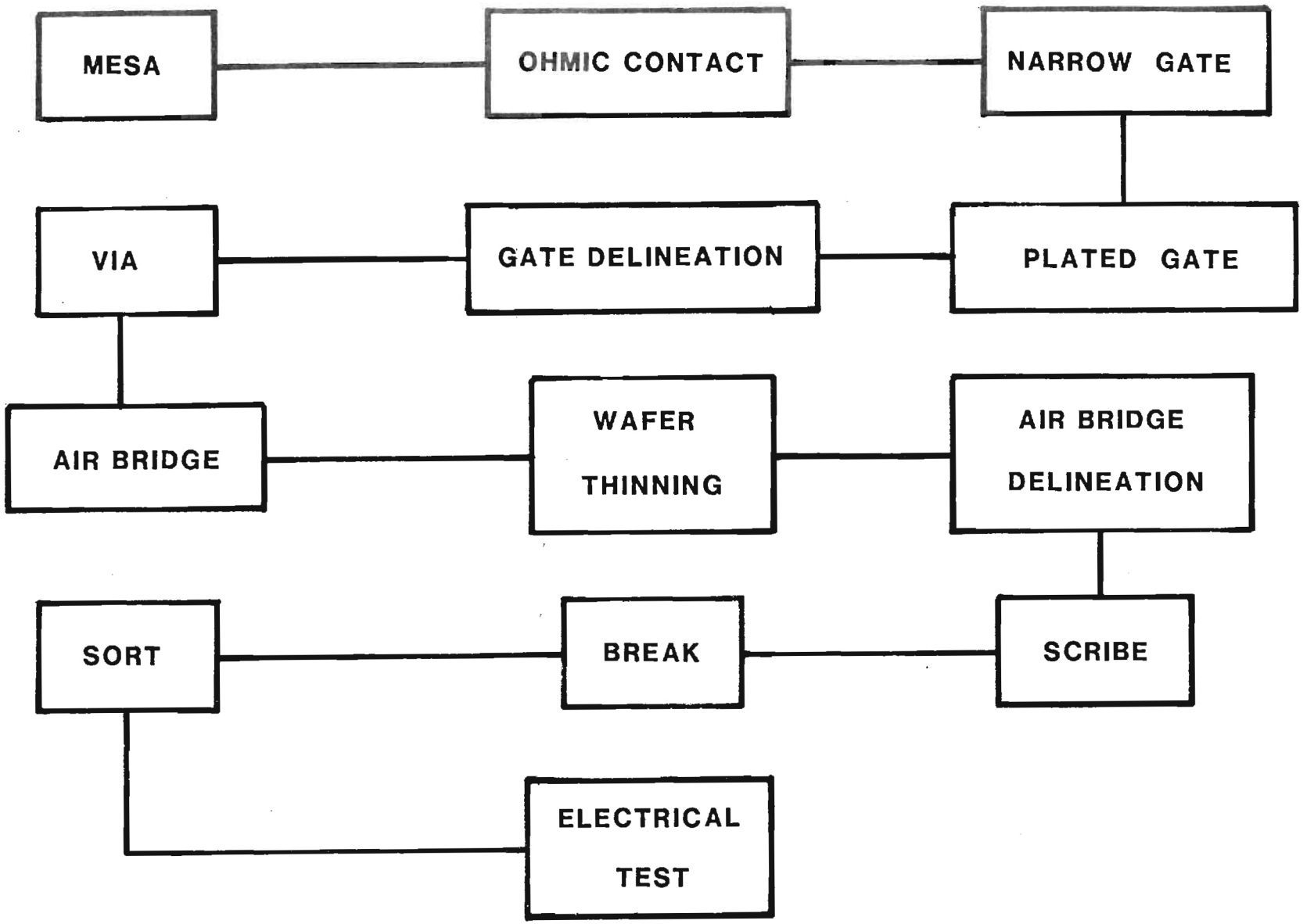


Figure 16. GaAs FET Fabrication Process

During wafer processing, it became evident that improvements could be made by altering the fabrication process in several areas. The mask set was designed such that ohmic contact definition was the first step. When processed in this manner, it was noted that the etchant used to etch GaAs during mesa formation degraded the GaAs/ohmic contact interface. Poor adhesion of the ohmic metallization was observed after mesa etch. The ohmic metallization is deposited prior to mesa formation to facilitate the determination of the point at which isolation is obtained during mesa etching. Once the height of the mesa is established for a given wafer, ohmic metallization is not necessary prior to mesa etch. On the latter wafer runs, mesa formation was performed prior to ohmic contact deposition with improved results.

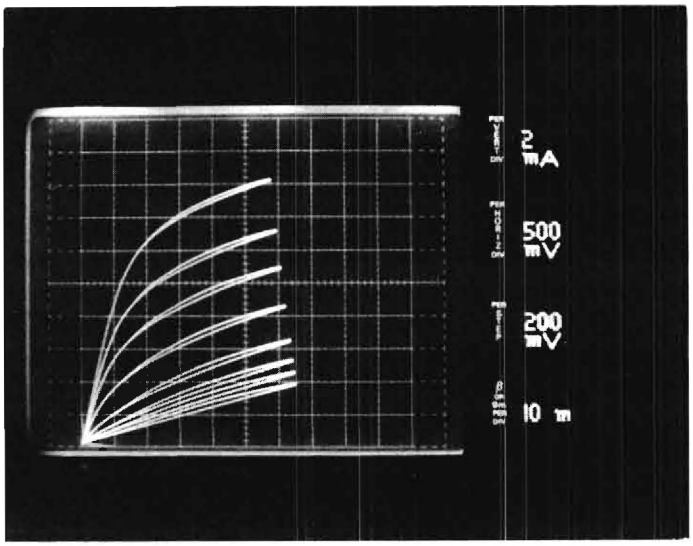
Rectangular wafer pieces 0.4 x 0.5 inches were used during process development. Photoresist build-up at the edges made it difficult to obtain uniform mask to wafer contact during exposure. To alleviate this problem, a mask was made of photographic film to allow the periphery of the wafer to be exposed. Subsequent development removed the photoresist around the edge of the wafer. Normal alignment and exposure were then possible, and improved results were obtained.

In order to improve the yield on air bridge devices, delineation of the air bridge was performed after wafer thinning. In this manner, photoresist under the air bridge provided structural support during the wafer thinning operation. After

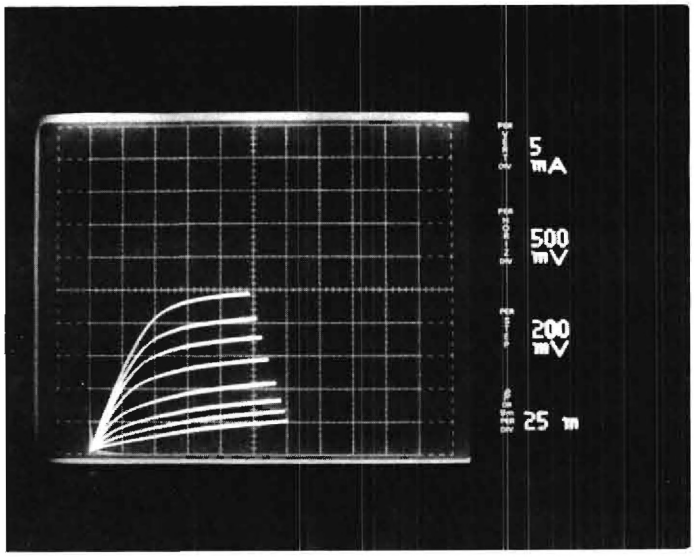
thinning the wafer, air bridge delineation was accomplished with no deleterious effects due to the lapping operation.

Improvement in the device transconductance has been observed as a result of heat treatment following wafer fabrication. Transconductance increases as large as 150% have been noted on devices which were heat treated at 460°C for 12 minutes. Various time and temperature conditions were evaluated, and the above values were found to be optimum. Heat treatment was performed in the furnace used for ohmic contact alloying. A forming gas ambient was utilized. Figure 17 shows the improvement in the I-V characteristics typically observed as a result of heat treatment. In addition to improved transconductance, the drain to source saturation current increases.

Figure 18 and 19 are SEM micrographs of a 0.5 x 150 micron FET from wafer 15H10-5. This wafer was processed with a lifted gate process, and the gate cross section is triangular. Figures 20 and 21 are micrographs of a 0.5 x 150 micron device from wafer 15I35-5. The complete fabrication process developed during this effort was used on this wafer run. Clearly visible in figure 21 is the thick gate structure.



(a) Before Annealing
0.5 x 150 μm



(b) After Annealing
0.5 x 150 μm

Figure 17. Current-Voltage Signatures Before and After Heat Treatment.

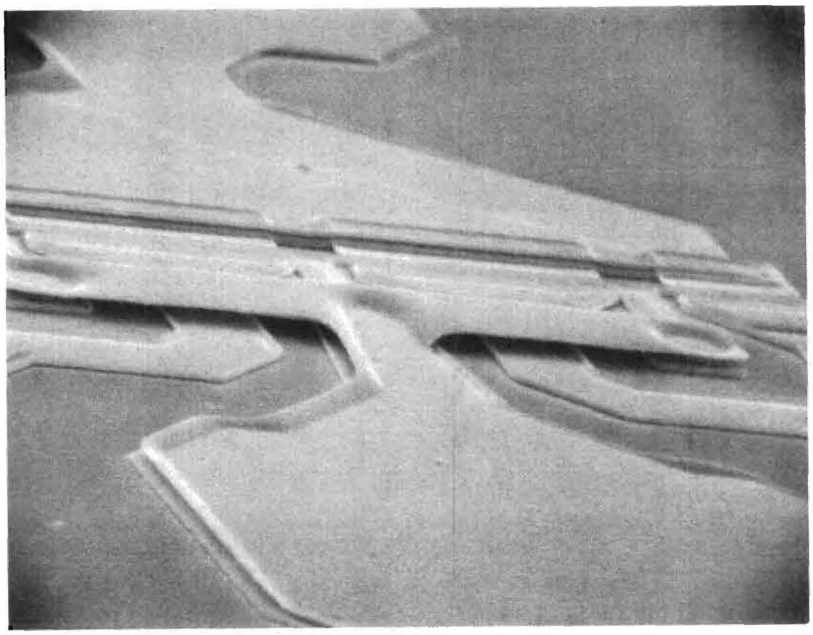


Figure 18. GaAs FET - 15H10-5

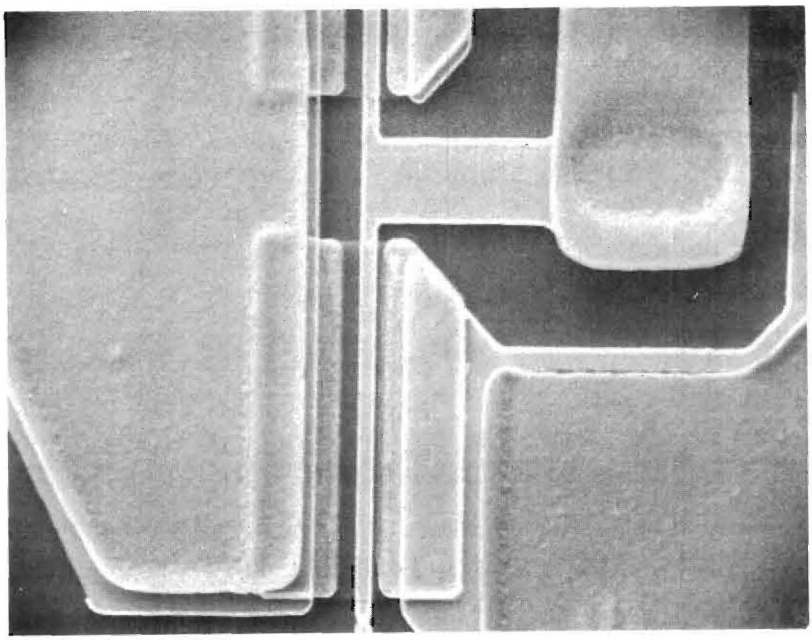


Figure 19. GaAs FET Gate Region -15H10-5

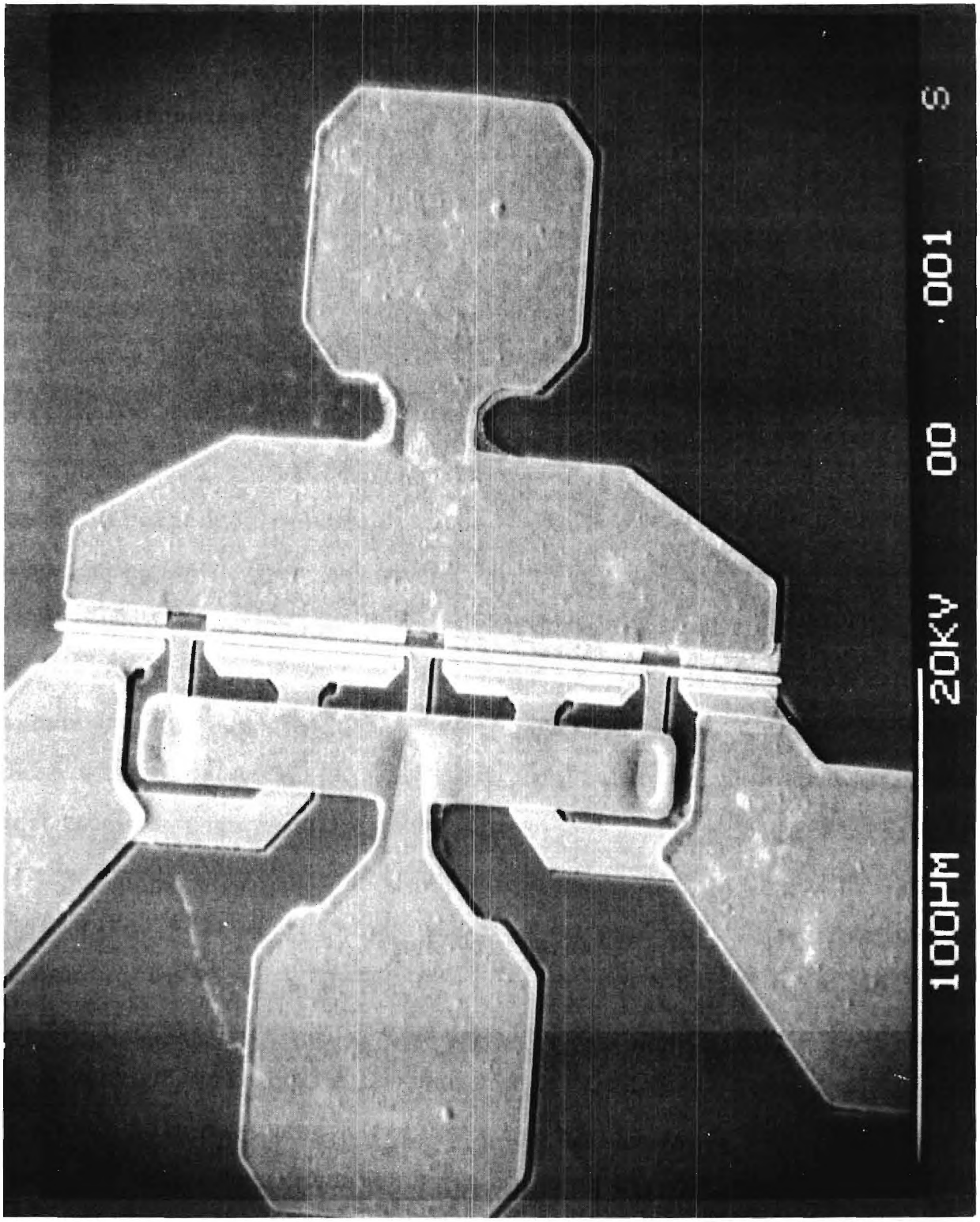


Figure 20. GaAs FET - 15I35-5

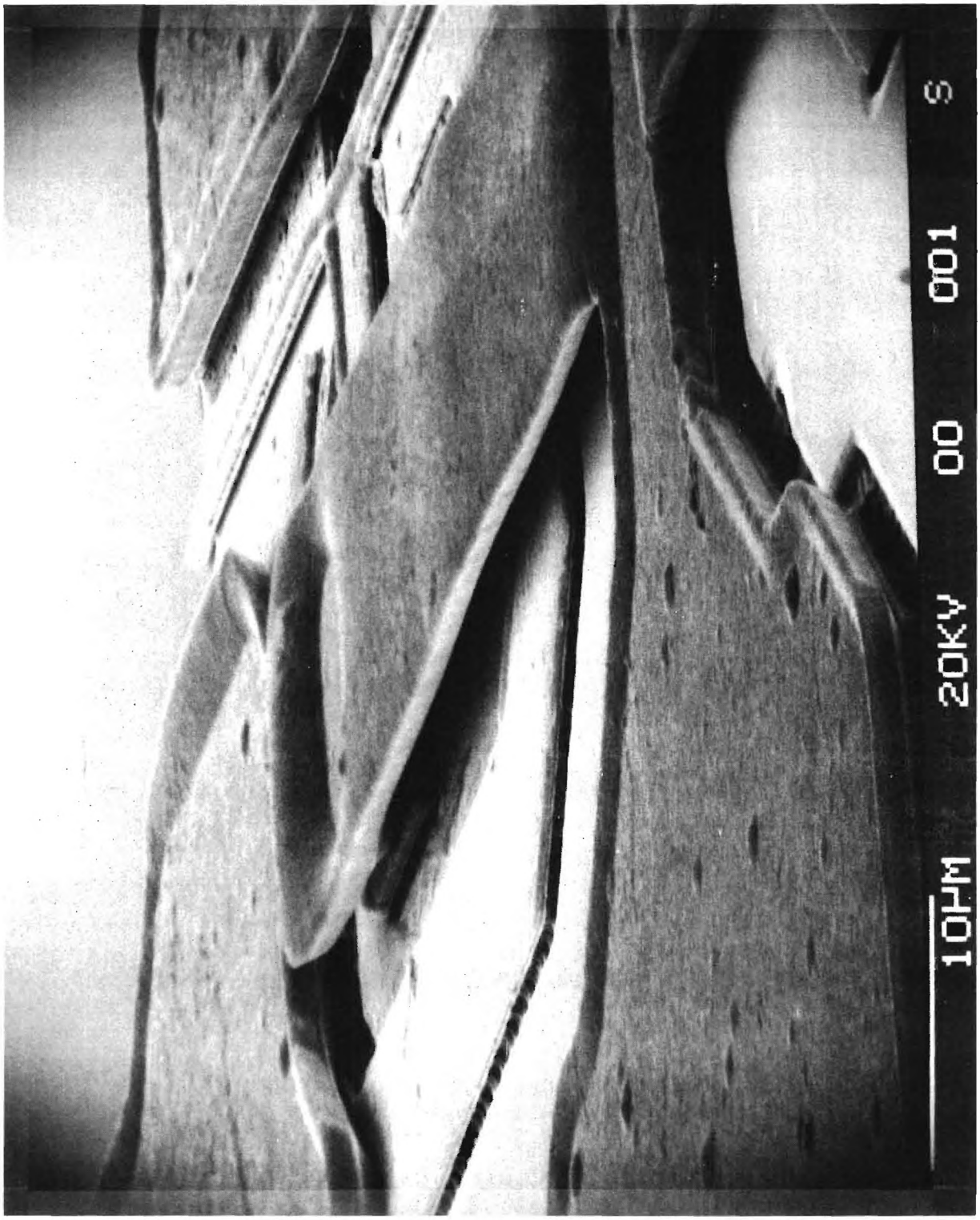


Figure 21. GaAs FET Air Bridge and Gate Region - 15I35-5

7.0 ELECTRICAL CHARACTERIZATION

7.1 DC Evaluation

DC characteristics were measured with a 4 probe test station, Tektronix 576 curve tracer, digital meters and power supplies. In addition to the measurements made at Georgia Tech, DC characteristics on run 15H10-5 were evaluated by Hughes using an HP 4145A Semiconductor Parameter Analyzer. Table 5 summarizes the results of the DC evaluation on four wafer runs. Wafer number 15I35-2 was not completely processed due to difficulties during gate delineation; however, limited data was obtained on several 1.0 micron gate length devices.

Figure 22 and 23 are curve tracer signatures typical of devices from runs 15H10-5 and 15I35-6 respectively. Probing between adjacent FETs on 15H10-5 disclosed leakage current on the order of 6 microamperes at 5 volts. This current, which is not controlled by the gate, reduces the transconductance and affects pinch off voltage.

Figure 24 is a graphics plot of data obtained with the HP Semiconductor Parameter Analyzer. Data can be rapidly obtained with this system and can be presented in a manner not possible with a conventional curve tracer.

Unity gain frequency (f_T) is a basic figure of merit for low noise GaAs FETs. This parameter is defined by the equation:

$$f_T = \frac{gm}{2\pi C_{gs}}$$

PARAMETER	15H10-5	I5I35-2	15I35-5	15I35-6	TEST CONDITION
Transconductance (mS/mm)	100	133	111	115	V_D = 3V, V_{GS} = 0V
Saturated Drain Current (mA/mm)	75 - 200	160 - 260	93 - 200	86 - 140	V_{DS} = 3V
Pinchoff Voltage (V)	-2V	-3V	-2.5	-2.5	V_{DS} = 3V, I_{DS} = 1 mA
Ideality Factor	1.2 - 1.4	1.4 - 1.6	1.2 - 1.35	1.2 - 1.35	

TABLE 5. DC CHARACTERISTICS

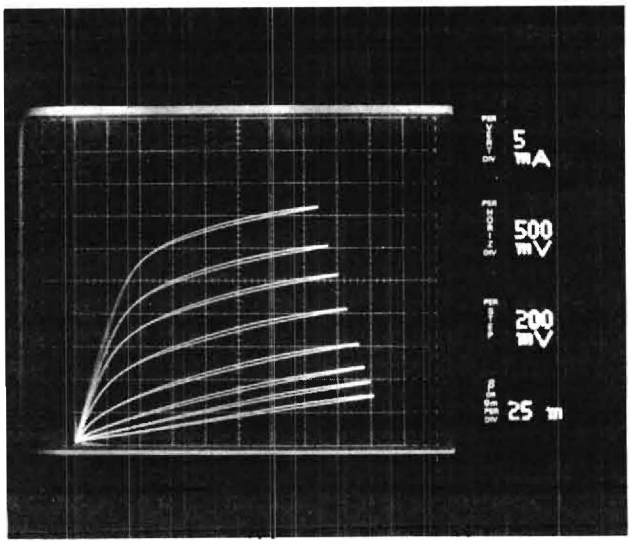


Figure 22. Curve Tracer Signature - 15H10-5.

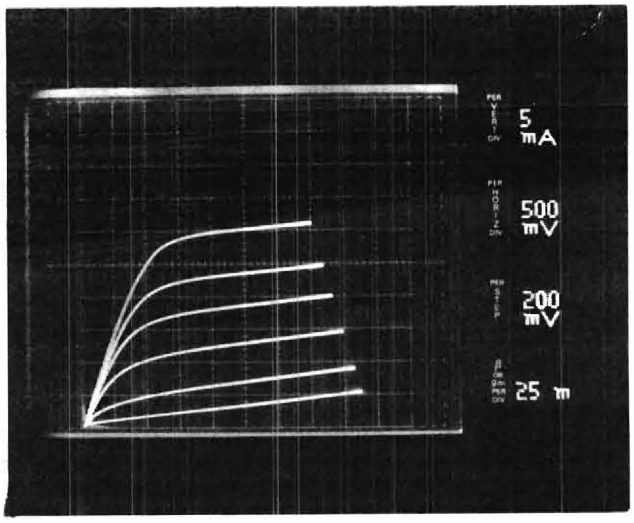


Figure 23. Curve Tracer Signature - 15I35-6.

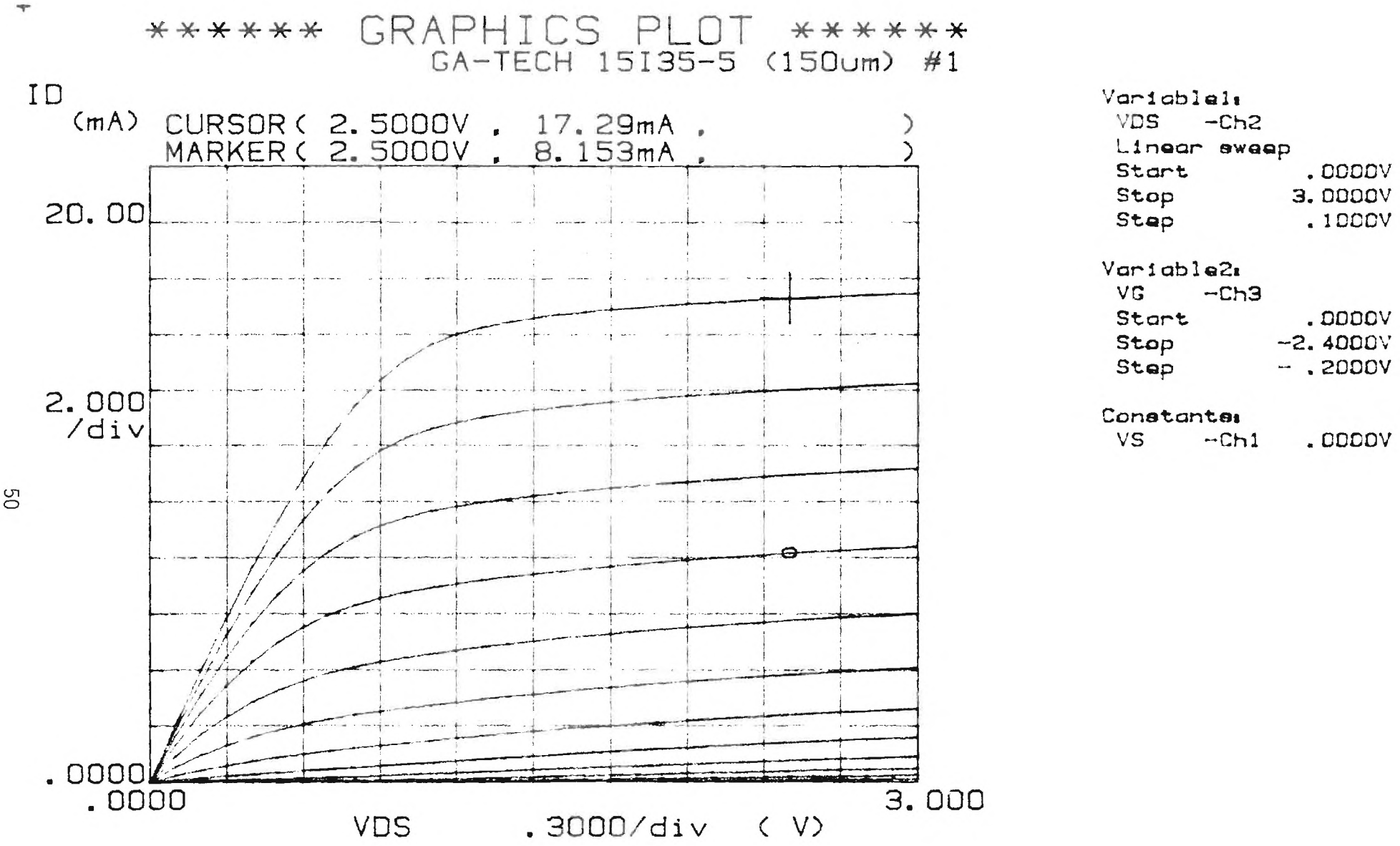


Figure 24. Graphics Plot 15I35-5

where g_m is the transconductance at a given gate voltage (V_{gs}) and C_{gs} is the gate to source capacitance at the same gate voltage.

Unity gain frequency can also be expressed in terms of gate length (L) by the equation

$$f_T = \frac{V_s}{2\pi L}$$

where V_s is the saturation velocity.
From the expression, it is clear that, for a given wafer, gate length is the single most important device parameter.

Unity gain frequency calculations were made on devices fabricated during this research by making point by point measurements of drain to source current (I_{ds}) and gate to source capacitance as a function of gate voltage. Drain to source voltage was maintained at 3 volts for I_{ds} measurements. No drain to source bias was applied during capacitance measurements.

Figure 25 is a plot of gate to source capacitance per unit gate length as a function of gate bias. Georgia Tech results are compared to the results obtained on commercial devices previously evaluated by this laboratory.[16] Figure 26 is a comparison of unity gain frequency as a function of gate to source bias. Gate lengths of devices used in this comparison are of nominally 0.5 micron design. However, SEM analysis of Georgia Tech devices indicated gate lengths on the order of 0.6 to .75 microns. Based

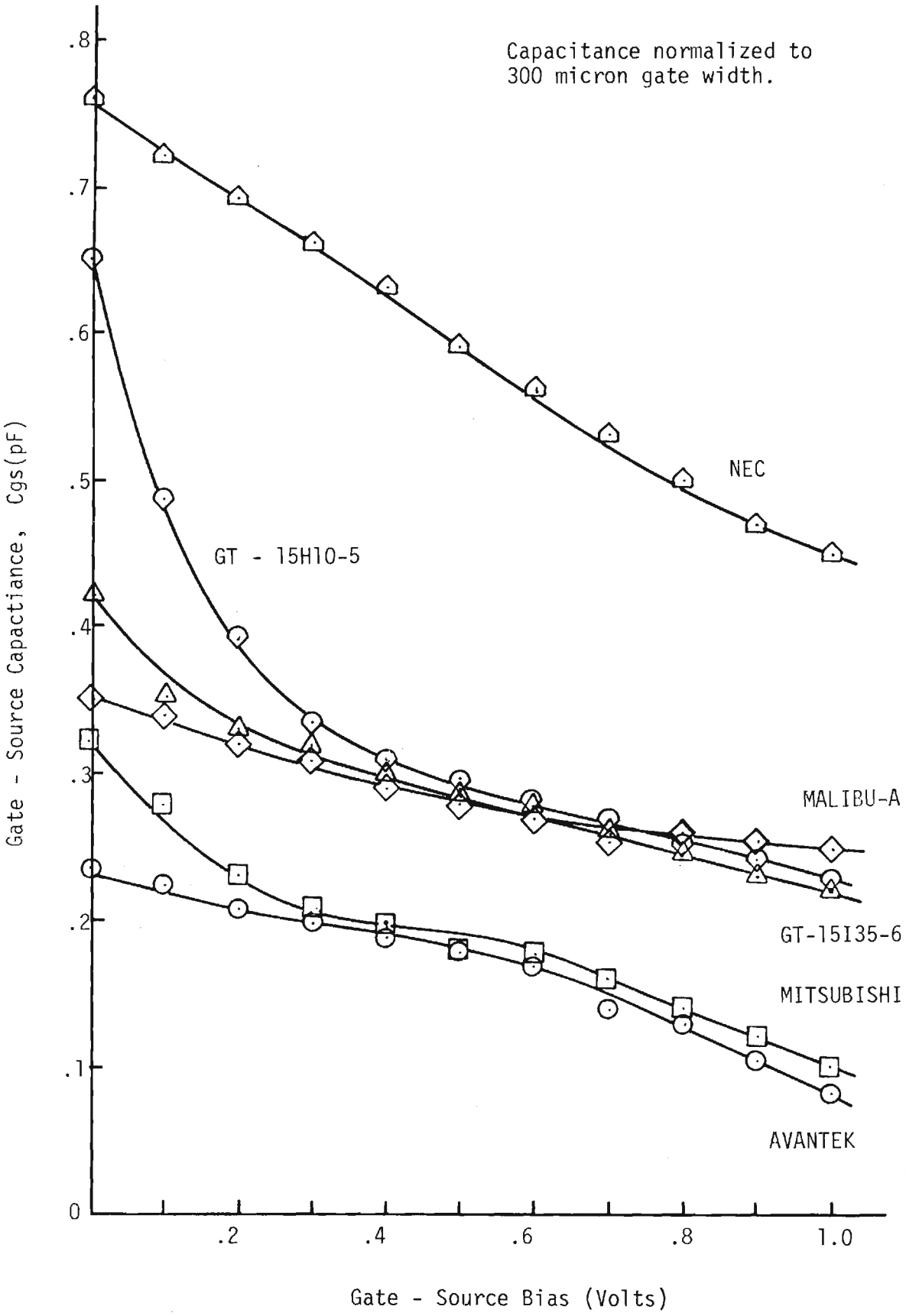


Figure 25. Gate Capacitance as a Function of Gate Bias.

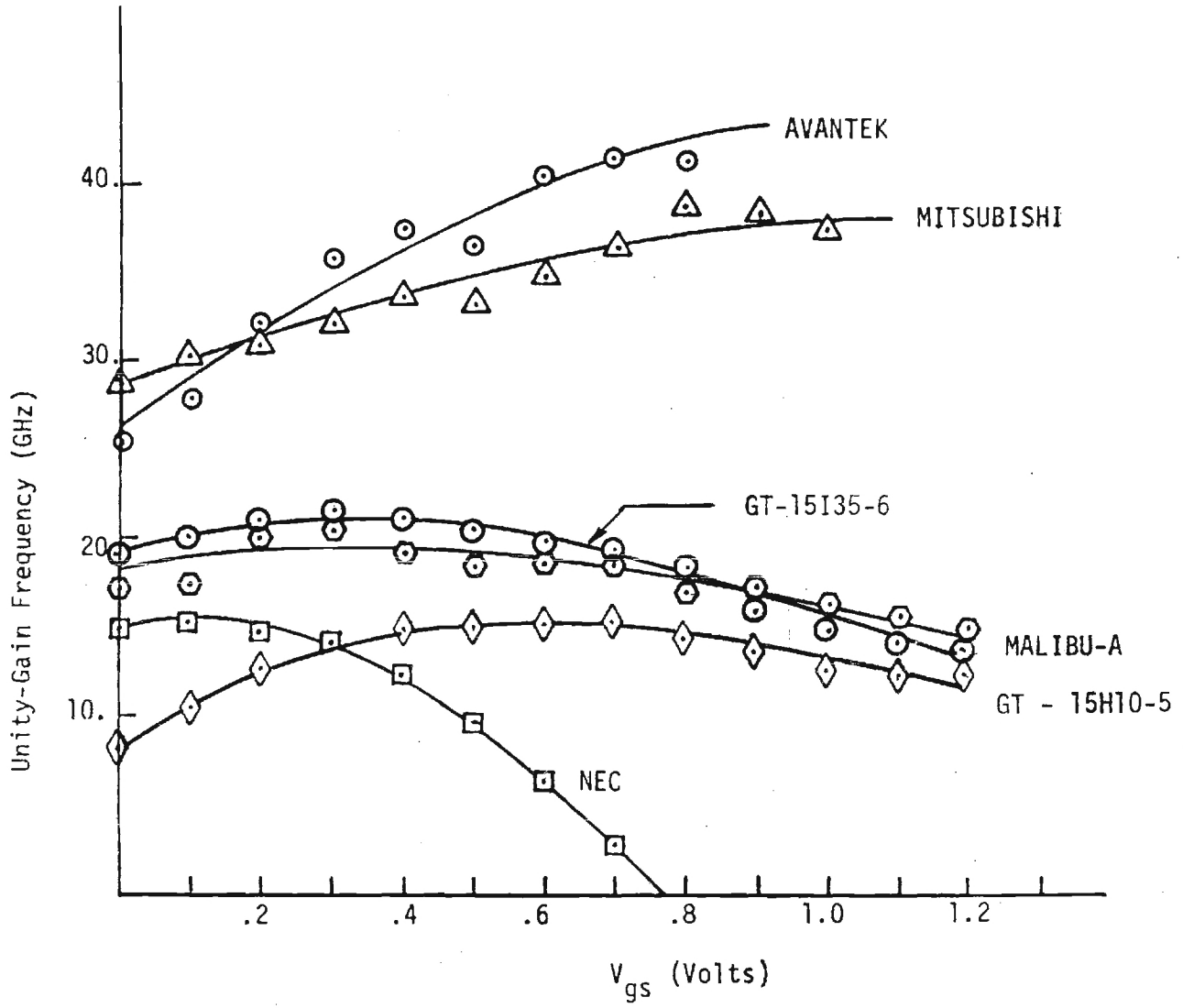


Figure 26. Unity-gain Frequency as a Function of Gate Bias.

on these data and the fact that improvements in the gate geometry are expected, encouraging results have been obtained during this research.

7.2 RF Test

Limited RF data have been obtained to date. Two devices from run 15H10-5 were measured by Hughes. RF gain was in the range of 3.0 to 3.5 dB over the frequency range of 11.7 to 12.3 GHz. Input power was - 2dBm. GaAs FETs having a gate width of 300 microns and gate lengths of 0.5 and 0.75 microns were tested. Bias conditions on the FETs were nominally:

V_{ds} = 3V

V_{gs} = -.8V

I_{ds} = 15-20 mA.

Better performance is expected on devices from runs 15I35-5 and 15I35-6.

7.3 Yield

Wafer 15H10-5 was fabricated with a lifted gate. Since the gate metal was sputter deposited, lift-off was difficult and some devices did not clear. Misalignment of the gate was also present on this run and the functional yield was on the order of 15%.

Wafer piece 15I35-5 had a functional yield of approximately 45% and was processed with the plated gate procedure. The wafer piece was from the edge of the master wafer, and surface imperfections were noted prior to device processing.

Wafer piece 15I35-6 had a functional yield of approximately 80%. This wafer piece came from the center of the master wafer

and had no apparent surface imperfections prior to processing. No process related difficulties were encountered on this run.

As this fabrication process matures, better device performance, more consistent performance and improved yields are expected, all of which are necessary for monolithic integrated circuit development.

8.0 SUMMARY AND CONCLUSIONS

A low noise GaAs FET fabrication process has been developed and refined to produce submicron gate length devices. This monolithic compatible process utilizes procedures and materials which should produce high performance, high reliability devices and circuits. Key design features include a plated gate structure and air-bridge interconnects. Specific tasks in this research effort included

- o Design and fabrication of a multi-layer mask set,
- o Specification and procurement of VPE epitaxial material,
- o Submicron photolithography,
- o Schottky barrier gate process development,
- o Ohmic contact studies,
- o Development of low-loss crossover interconnects,
- o Device fabrication and
- o Device characterization.

A seven level mask set composed of an array of FETs was designed using the Georgia Tech Microelectronic Research Center computer aided design system. Diagnostic structures were included to aid process development and process control. Masks were fabricated by Micro Mask Inc. using chrome on LEU glass plates. Patterning was performed by direct write electron beam exposure.

As in other monolithic IC processes, multiple photolithographic steps are required in this fabrication process. A Karl Suss MJB3/HP Mask Aligner, fitted with 310 nanometer

optics, was used to expose Microposit 1350J photoresist. Different resist viscosities were used at various steps to achieve the desired thicknesses. Faithful delineaton of the 0.5 micron gate length geometries was difficult to obtain.

The most difficult area of process development was the removal of the excess metal and resist after electroplating the gate. Considerable time and effort was expended in determining chemicals and processes which would remove the undesired materials without deleteriously affecting the GaAs. H_2O_2 was found to be best for removing the Ti/W metallization. Underlying photoresist was successfully removed with a combination of a commercial solvent and an oxygen plasma.

Two wafer runs were processed through all fabrication steps with reasonable device yield. Device transconductances were on the order of 120 mS/mm. Typical unity gain frequency of these devices was on the order of 18 GHz with values as high as 25 GHz noted on selected devices.

Based on this research effort, the development of monolithic GaAs ICs using this basic process for the GaAs FET active devices is feasible and is a logical next step. Performance improvements are expected as the process matures and as better materials, masks, and photoresist techniques evolve.

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APPENDIX A

GaAs FET PROCESS CHECKLIST

Date Started _____ Wafer No. _____

Date Completed _____ Size _____

Thickness _____

REFERENCES:

GaAs FET Process Instructions
Hughes FET Array Mask Set
A-3459 and A-3814 Monthly Reports
Final Report Project A-3459

	PROCESS	P.I. No.	STATUS Completed	Problem
1.	GaAs material	PI-0	[ ]	
2.	Scribe and break	PI-1	[ ]	
3.	Wafer map	PI-1	[ ]	
4.	Clean	PI-1	[ ]	
5.	Inspect	PI-1	[ ]	
6.	Mesa photoresist	PI-2	[ ]	
7.	Inspect	PI-2	[ ]	
8.	Post bake	PI-2	[ ]	
9.	Mesa etch	PI-2	[ ]	
10.	Strip photoresist	PI-2	[ ]	
11.	Inspect	PI-2	[ ]	
12.	Bake	PI-3	[ ]	
13.	Ohmic contact photoresist	PI-3	[ ]	
14.	Clorobenzene soak	PI-3	[ ]	
15.	Bake	PI-3	[ ]	
16.	Develop	PI-3	[ ]	
17.	Inspect	PI-3	[ ]	
18.	GaAs clean	PI-4	[ ]	
19.	Ohmic contact evaporation	PI-4	[ ]	
20.	Lift-off	PI-4	[ ]	
21.	Alloy	PI-4	[ ]	
22.	Gate photoresist	PI-5	[ ]	
23.	Inspect	PI-5	[ ]	
24.	Post bake	PI-5	[ ]	
25.	SEM	PI-5	[ ]	
26.	Gate recess	PI-5	[ ]	
27.	Clean	PI-6	[ ]	
28.	Gate deposition	PI-6	[ ]	
29.	Plated gate photoresist	PI-7	[ ]	

30. Gold electroplate	PI-8	[ ]
31. Gate definition	PI-9	[ ]
32. Electrical test	PI-10	[ ]
33. Clean	PI-11	[ ]
34. Via photoresist	PI-11	[ ]
35. Thin Film depostion	PI-12	[ ]
36. Air bridge photoresist	PI-13	[ ]
37. Gold electroplate	PI-14	[ ]
38. Wafer thinning	PI-15	[ ]
39. Air bridge definition	PI-16	[ ]
40. Scribe and break	PI-17	[ ]
41. Clean	PI-17	[ ]
42. Sort	PI-18	[ ]
43. Electrical test	PI-10	[ ]

APPENDIX B

PROCESS INSTRUCTIONS

SCOPE

To specify epitaxial gallium arsenide wafer material.

APPLICABLE DOCUMENT

Contract No. S8-879406-LPY

REQUIREMENTS

1. Gallium arsenide substrate characteristics to be supplied as required.

   a. Boule supplier, Boule number and wafer number
   b. Orientation, 2° off < 100 > toward < 110 >
   c. Dopant, Cr or Undoped
   d. Resistivity, > 10^{7} ohm-cm
   e. Area, as required, typically 16-18 cm^2

2. Gallium arsenide buffer layer characteristics

   a. Carrier concentration < 10^{14} cm^{-3}
   b. Thickness > 2 microns

3. Gallium arsenide active layer characteristics

   a. Dopant, silicon
   b. Carrier concentration, 2.0×10^{17} to 3.0×10^{17} cm^{-3}
   c. Thickness, 0.15, to 0.22 microns
   d. Doping concentration shall fall from nominal carrier concentration to 1×10^{17} cm^{-3} over less than 250 angstroms and shall fall from 1×10^{17} cm^{-3} to the buffer layer conc. over less than 750 angstroms.

QUALITY ASSURANCE PROVISIONS

4. Inspect surface morphology

   a. Surface haze
   b. Hillocks
   c. Cracks

5. Data sheets

   a. Impurity profile
   b. Vendor quality assurance document

SCOPE

To describe GaAs wafer preparation prior to mesa photolithography.

APPLICABLE DOCUMENT

Contract Number S8-879406-LPY

REQUIREMENTS

1. Equipment

   a. Wafer scriber
   b. Wet chemical fume hood
   c. Hot plate, HPA1915B
   d. Microscope, 50-100X, Bausch and Lomb
   e. Sonic cleaner, model 75, Beuhler Ltd.
   f. Mazur lapping machine, model 601
   g. Lapping fixture
   h. Thickness gauge
   i. Pneumatic pressure fixture

2. Chemicals and supplies

   a. Dry nitrogen gas
   b. Deionized water, filtered
   c. Methanol, electronic grade
   d. Trichloroethylene, electronic grade
   e. Microstrip, solvent
   f. Paraffin wax
   g. Silicon carbide powder, 1000 grit
   g. Miscellaneous supplies:
      tweezers, tri-grip teflon holder, petri dishes, beakers, filter paper, kimwipes and lens paper

PROCEDURE

1. Scribe and break wafer

   a. Carefully remove GaAs wafer from storage container.
   b. Scribe and break to yield wafer = 0.5 x 0.5 inches

2. Wafer map

a. Make diagram of the entire wafer.
b. Indicate on diagram location of wafer piece.

3. Wafer Clean

a. Grip wafer with tri-grip telfon holder.
b. Prepare beaker of tricholorethylene and immerse wafer. Sonic agitate beaker for 1 minute.
c. Prepare a second beaker of trichlorethylene. Heat to boiling. Immerse wafer into vapor for 30 seconds.
d. Rinse wafer in methanol followed by rinse in running DI water.
e. Blow dry using N_2 opposed jet dryer.
f. Immerse in microstrip (40 ml.) for 30 seconds.
g. Rinse in methanol for 30 seconds.
h. Spray with methanol 10 seconds.
i. Blow dry using N_2 opposed jet dry.

4. Inspect

a. Inspect surface with a microscope by observing reflected light from the wafer.
b. Place wafer in a clean, covered petri dish.
c. Label dish cover to retain wafer identity.

5. Wafer Lapping [OPTIONAL - Perform only if wafer is not flat]

a. Place the lapping mandrel on thickness gauge and zero the gauge.
b. Remove mandrel and place it on the hot plate set at 90°C.
c. When the side of the mandrel is uncomfortably warm, remove it and apply a small amount of wax to the mounting surface.
d. Quickly lay the wafer face down in the wax and place a 1" square piece of lens paper over the wafer.
e. Place the mandrel in the pneumatic pressure stand and center under diaphram. Lower diaphram holder and turn on the air supply.
f. When cool, release the air pressure and remove the lapping mandrel. Remove excess wax with a cotton swab and tricholorethylene.
g. Prepare lapping slurry by sprinkling 1/4 teaspoon of 1000 grit onto glass flat of the lapping machine and adding deionized water.
h. Insert mandrel into the lapping fixture holder and set holder into the lapping tray. Move holder around by hand to distribute the grit. Set speed control to 1/2 speed and turn on machine.
NOTE: Material removal rate may vary. Check thickness often. Terminate lapping when wafer thickness is = 15 mils.

6. Wafer removal and cleaning

a. Swab edges with tricholorethylene to remove all traces of grit.
b. Immerse mandrel in a beaker of boiling DI water to remove the wafer.
   NOTE: Use extreme care to avoid scratching wafer surface.
c. Pour off water and flood with methanol. Pour off methanol and flood with trichloroethylene. Flood with methanol once again.
d. Rinse in running hot DI water for 3 minutes.
e. Carefully remove from beaker and blow dry with N_2.
f. Place in clean covered petri dish.

SCOPE

To describe the procedures necessary for mesa isolation.

APPLICABLE DOCUMENTS

Contract Number S8-879406-LPY
Suss MJB3 Mask Aligner Operator's Manual

REQUIREMENTS

1. Equipment

   a. Photoresist spinner, model no. AHT2A-T, Headway Research, Inc.
   b. Temperature and humidity controlled glove box for spinner.
   c. Ovens, fresh air convection, 95°C and 110°C.
   d. Mask aligners, model No. 686B Kulicke & Soffa and model no. MJB3/HP, Karl Suss.
   e. Microscope, 100X to 800X magnification, Unitron, model no. TMS-6560.
   f. Alpha-step profiler, Tencor

2. Chemicals and Supplies

   a. Positve photoresist, Microposit 1350J, thinned 3 parts resist to 1 part thinner
   b. Photoresist thinner, Microposit thinner
   c. Developed, Microposit 351
   d. DI water
   e. N_2 gas
   f. Beakers, hold-down wand, tweezers, tri-grip holder, etc.
   g. Acetone, electronic grade
   h. Phosphoric acid - 85%
   i. Hydrogen Peroxide - 30%
   k. Microposit remover 140 - Shipley
   l. Propanol

PROCEDURE

1. Apply Photoresist - preset speed: 6000 RPM, time 25 secs.

   a. Remove wafer from container.
   b. Place wafer on spinner chuck and turn on vaccum.
   c. Apply thinned AZ1350J resist, start spin immediately.
   d. Release vacuum, remove wafer and place in petri dish lined

with filter paper.

2. Softbake

   a. Remove wafer from petri dish and place in convection oven set at 95 + 5°C.
   b. Bake for 25 minutes.

3. Expose and develop edges

   a. Cover center of wafer with opaque photographic film mask.
   b. Clamp in place with glass slide.
   c. Expose with Kulicke & Soffa mask aligner for 5 sec.
   d. Develop in Microposit 351 developer:DI water 1:3 1/2 for 30 seconds.
   e. Rinse 2 minutes in DI water.
   f. Dry with N_2 gas.

4. Align and Expose

   a. Turn on mask aligner. Allow to warm up for at least 15 minutes.
   b. With white nylon gloves, CAREFULLY remove mesa mask from the storage container. Inspect the surfaces for photoresist residue and dust. Blow off dust with N_2. If photoresist residue is present, perform step c.
   c. Mask cleaning. Put on rubber gloves. Place 3 drops of Joy detergent in 2000 ml beaker and fill with 800 ml. of DI water. Remove mask from storage container and rinse with acetone followed by methanol, then DI water. Place in detergent solution and agitate for 30 seconds. Rinse in hot DI 30 seconds. Blow dry.
   d. Place mask on frame holder.
      TURN ON VACUUM.
   e. Place mask/frame assembly on mask aligner and tighten clamps.
   f. Place wafer on wafer chuck and slide into position.
   g. Bring wafer into contact with mask by turning the contact lever counterclockwise.
   h. The contact light should be on at this time.
   i. Pull the separation lever toward the front of the machine to obtain sufficient separation for alignment.
   j. Use the X, Y, and theta micrometers to align the wafer to the mask.
   k. Press the buttons on the microscope manipulator to scan in the X and Y directions.
   l. When satisafactory alignment has been obtained, push the separation lever to its rear most position. The contact light will re-illuminate.
   m. Press the chamber vacuum button located on the side of the machine and reinspect the alignment.

n. Set the timer for 22 seconds.
NOTE: THIS TIME IS FOR THE MESA LEVEL ONLY. OTHER LEVELS REQUIRE DIFFERENT TIMES.
o. Press the expose button
NOTE: STAND CLEAR OF THE MICROSCOPE
p. After exposure is completed, rotate contact level clockwise to lower wafer.
q. Slide wafer out of alignment stage.
r. Carefully remove wafer from wafer chuck and place in covered petri dish.
s. Loosen mask holder clamps and remove mask holder assembly.
t. Turn mask vacuum off.
u. With white nylon gloves, remove mask and return it to its storage container.
v. Turn off mask aligner (depending on requirements).

5. Develop Photoresist

a. Mix developer 1 part Microposit 351 to 3.5 parts DI H_2O. In a separate 250 ml beaker decant DI H_2O for rinsing.
b. Place wafer on vacuum hold-down wand.
c. Immerse in developer for 30 seconds.
d. Rinse immediately in DI H_2O beaker for 30 seconds.
e. Rinse an additional 30 seconds in running DI H_2O.
f. Blow dry using dry nitrogen gas.

6. Inspect

Inspect the images formed by the process at low magnification (100X) for gross anomalies. Using high magnification, inspect the patterns for edge acuity and complete resist removal in the pattern areas. Scan the entire wafer to ensure pattern uniformity. If residual photoresist is observed or patterns are not well defined, contact process engineer.

7. Post Bake

a. Place wafer on filter paper and insert in fresh air convection oven at 110°C.
b. Bake for 10 minutes.
c. Remove and place in covered petri dish.

8. Mesa Etch

a. Prepare H_3PO_4:H_2O_2:H_2O solution using 3 ml. H_3PO_4, 1 ml. H_2O_2 and 50 ml. H_2O. Also prepare 75 ml. of wetting solution by placing one drop of Microclean in beaker of DI. Pour and refill several times to make dilute solution. Also prepare rinse beaker of DI water.

b. Place beaker of etchant (3:1:50) in constant temperature bath and allow to stabilize to 22 ± 2°C.
c. Measure photoresist thickness using Tencor step profiler.
d. Using tri-grip holder, immerse wafer in wetting solution for 2 seconds.
e. Immerse in 3:1:50 etchant for one minute.
f. Rinse immediately.
g. Rinse in running DI H_2O for one minute.
h. Blow dry with N_2.
i. Measure thickness with step profiler.
j. Repeat steps d through h using successively shorter times until a mesa height of 0.25 microns is achieved.
NOTE: Mesa height is dependent on active layer thickness. Check wafer quality assurance data prior to etching.

9. Strip Photoresist

a. Decant 40 ml. of Microposit 140 Remover into a 100 ml. beaker. Heat to 50°C.
b. Immerse wafer in remover and agitate for 5 minutes.
c. Rinse with propanol.
d. Rinse with methanol.
e. Rinse with hot DI H_2O.
f. Blow dry with N_2.

10. Inspect

a. Using low magnification, inspect wafer by observing reflected fluorescent light.
b. Also inspect at high magnification.
c. Repeat microposit remover soak if necessary.
d. Place wafer in covered petri dish.

SCOPE

To describe steps involved in patterning the wafer for ohmic contact metallizaton.

APPLICABLE DOCUMENT

Contract Number S8-879406-LPY

REQUIREMENTS

1. Equipment
   a. Photoresist spinner
   b. Glove box for spinner
   c. Ovens, fresh air connection, 80°C, 95°C and 110°C
   d. Mask aligners, model No. 686B, Kulicke and Soffa and model no. MJB3/HP Karl Suss.
   e. Microscope, 100X to 800X magnification, Unitron, Model No. TMS-6560.

2. Chemicals and Supplies

   a. Positive photoresist, Microposit 1350J thinned 3:1
   b. Developer, Microposit 351
   c. DI water
   d. N_2 gas
   e. Chlorobenzene
   f. Beakers, hold-down wand, tweezers, tri-grip holder, etc.

PROCEDURE

1. Bake

   a. Obtain wafer from PI-2.
   b. Bake at 110°C 10 min.
   c. Remove and place in covered petri dish.
   d. Place on vacuum wand and clean with N_2 gas.
   e. Return wafer to petri dish and transport to photoresist spinner.

2. Ohmic Contact Photoresist

   a. Apply photoresist according to PI-2.
      Resist - 3:1 1350J
      Speed - 6000 RPM

Time - 25 seconds

b. Return wafer to petri dish
c. Air dry 10 minutes
d. Remove wafer from petri dish, place on filter paper and insert in softbake oven.
e. Bake at $95^{o}C \pm 2^{o}C$ for 25 minutes
f. Turn on K&S and Karl Suss mask aligners while wafer is in soft bake.
g. Remove wafer from oven and allow to cool 3 minutes.
h. Expose and develop edges as in PI-2 using K&S aligner.
i. Dry in N_2 gas.
j. Return to petri dish.
k. Install ohmic mask in Suss mask aligner observing cautions in PI-2.
l. Align mask to previous pattern.
m. Expose 22 sec.
n. Remove wafer and place in petri dish.
o. Remove mask and return it to storage container.

3. Chlorobenzene Soak

a. In a fume hood, pour 40 ml of chlorobenze in a 100 ml beaker. Cover with a watch glass.
b. Remove wafer from petri dish and insert in tri-grip holder.
c. Remove watch glass from chlorobenzene and immerse wafer for 6 min.
d. Remove wafer from chlorobenzene and place on vacuum wand.
e. Immediately dry with N_2 gas.
f. Return wafer to petri dish.

4. Bake

a. Remove wafer from petri dish and place on filter paper
b. Place in $80^{o}C$ oven and bake for 5 minutes.
c. Remove from oven and return to petri dish.

5. Develop Photoresist

a. Mix 1 part of developer with 3.5 parts DI H_2O as is PI-2.
b. Prepare rinse beaker
c. Place wafer on vacuum hold-down wand
d. Immerse in developer for 55 seconds.
e. Rinse immediately in DI H_2O beaker for 30 seconds.
f. Rinse an additional 30 seconds in running DI H_2O.
g. Blow dry using dry nitrogen gas.

6. Inspect

Inspect images as in PI-2.

GEORGIA TECH ENGINEERING EXPERIMENT STATION

Drain Source
Ohmic Contact

PROCESS INSTRUCTION FOR GaAs FET

PI-4

SCOPE

To describe steps involved in depositing, patterning and alloying AuGe-Ni-Au metallization for drain and source contacts.

APPLICABLE DOCUMENT

Contract Number S8-879406-LPY

REQUIREMENTS

1. Equipment

   a. Vacuum evaporator, Veeco model 775
   b. Wet chemical fume hood
   c. Alloy furnace
   d. Hot plate, 60°C
   e. Vacuum hold-down wand

2. Chemicals and Supplies

   a. Ammonium hydroxide, reagent grade
   b. Acetone
   c. Trichloroethylene
   d. Metals (Marz grade or better)
      AuGe (88/12)
      Ni
      Au
   e. Dry N_2
   f. LN_2
   g. Forming gas mixture, 90% N_2, 10% H_2
   h. Miscellaneous supplies - beakers, tweezers, tri-grip holder

PROCEDURE

1. Prepare vacuum evaporator

   a. Fill cold trap with LN_2
   b. Switch from "lock standby" to "automatic"
   c. Press start button
   d. Pump to $< 1 \times 10^{-6}$ torr.
   e. Clean boats by setting current to 200A and heating for

30 seconds. Clean boats sequentially in the order Au, Ni then AuGe.

f. Turn off current and allow boats to cool.

g. Weigh out
   22 mg AuGe
   3 mg Ni
   30 mg Au
   all Marz Grade or better.

h. Degrease all charges in boiling trichloroethylene vapor. Transport to vacuum evaporator.

2. GaAs Clean

a. In a wet chemical fume hood, mix 5 ml of ammonium hydroxide with 50 ml of DI H_2O (room temp). Prepare a rinse beaker with 200 ml of deionized water.

b. Remove wafer from petri dish and, using trip-grip teflon holder, immerse wafer for 10 seconds. Immediately rinse in DI water. Perform final rinse in running hot DI water for 15 seconds.

c. Dry using opposed jet N_2 blow station.

d. Place dried wafer into clean petri dish and transport to vaccum evaporator.

3. Load Wafer and Charges

a. Press stop button, system will vent and raise bell-jar automatically.

b. Remove substrate holder from chamber. Mount wafer under spring clips using care not to shield the alignment marks with the spring clips. Replace holder.

c. Remove the boat shield.

d. Place AuGe alloy charge into center tungsten boat. Place Ni charge in farthest boat. Place Au charge in front boat.

e. Replace shield.

f. Press start button. System will automatically lower bell jar and pump down.

4. Evaporate charges

a. Melt charges by sequentially heating Au at 100 Amps, Ni at 150 Amps and AuGe at 100 Amps until each charge just melts.

b. Let cool 30 seconds.

c. Deposit AuGe by bringing up current slowly. After AuGe melts, open shutter and bring current up to 150 Amps. Maintain at 150 Amps for 4 seconds after opening shutter. Close shutter and reduce current. Allow to cool 10 seconds. Repeat process until charge is completely evaporated.

d. Switch to Ni boat. Bring current up slowly, as melting begins, open shutter and turn current up to 200 Amps.

Maintain for 4 seconds. Close shutter and reduce current. Allow to cool 10 seconds. Repeat until charge is completely evaporated (6 cycles).

e. Switch to Au boat. Repeat as in C above.
f. Allow to cool 5 minutes
g. Press stop.
h. When bell-jar raises, remove substrate holder.
i. Remove wafer from holder using care not to damage the alignment patterns.
j. Replace substrate holder.
k. Press start button.
l. Return system to "lock standby" after 20 minutes of pumping.

5. Lift-off

a. Decant 50 ml. of acetone into 100 ml beaker
b. Immerse wafer in acetone.
c. Place on hot plate 60°C and agitate lightly.
d. After excess metal has completely lifted, pour off acetone.
e. Rinse with fresh acetone. Pour off.
f. Rinse with methanol. Pour off.
g. Rinse with DI water. Remove and rinse in hot running DI water.
h. Dry with N_2 gas.

8. Alloy

a. Set alloy platen temperature to 425°C.
b. Open forming gas valve and set flow to full scale. Slide furnace tray out of furnace and place the wafer on the tray. Return try to preheat position.
c. Reduce forming gas flow to a reading of 10. Allow furnace to purge for 3 minutes.
d. Push tray into hot zone. Turn on quartz lamp for 10 seconds. Leave wafer on platen for a total of 30 seconds, slide furnace tray to the preheat position.
e. Remove tray after 15 seconds. Slide wafer onto clean filter paper in petri dish.
f. Turn off forming gas.

SCOPE

To describe the procedure for delineating the gate region and performing recess etch.

APPLICABLE DOCUMENTS

Contract S8-879406-LPY
Process Instruction PI-2

REQUIREMENTS

1. Equipment

   a. Photolithographic equipment listed in PI-2
   b. Ovens, fresh air convection, 95°C and 110°C.
   c. Scanning Electron Microscope, Cambridge model stereo scan 150 or equivalent.
   d. Tektronix 576 curve tracer
   e. Probe station
   f. SEM holder

2. Chemicals and Supplies

   a. Positive photoresist, microposit 1350J, thinned 2 parts resist to 1 part thinner
   b. Developer, Microposit 351
   c. DI water
   d. N_2 gas
   e. Phosphoric acid - 85%
   f. Hydrogen peroxide - 30%
   g. Beakers, hold-down wand, tweezers tri-grip holder, etc.
   h. Microclean, surfactant

PROCEDURE

1. Clean wafer

   a. Obtain wafer from PI-4.
   b. Place on vacuum wand.
   c. Clean surface with N_2 gas.
   d. Place in covered petri dish.

2. Gate Photoresist - preset speed: 6000 RPM, time 25 sec.

a. Remove wafer from container
b. Place wafer on spinner chuck and turn on vacuum.
c. Apply 2:1 photoresist and spin immediately.
d. Release vacuum, remove wafer, place in petri dish partially covered and air dry 10 minutes.
e. Soft bake at 95°C for 25 minutes.
f. Turn on both mask aligners while wafer is baking.
g. Remove wafer from softbake oven.
h. Allow to cool 3 minutes
i. Expose and develop edges as in PI-2.
j. Dry in N_2 gas.
k. Return to petri dish.
l. Install narrow gate mask in Suss aligner observing cautions in PI-2.
m. Align mask to previous pattern. Note: Slight offset is necessary for proper alignment. Consult process engineer.
n. Expose 24 seconds.
o. Develop for 25 seconds.
p. Rinse immediately in DI H_2O beaker for 30 seconds
q. Rinse in running DI H_2O for 30 seconds.
r. N_2 dry.
s. Return to petri dish.

3. Inspect

Inspect images as in PI-2.

4. Post bake

a. Remove wafer from petri dish and place on filter paper.
b. Bake at 110°C for 10 minutes.
c. Remove wafer and return to covered petri dish.

5. SEM

a. Mount wafer on SEM holder.
b. Transport in covered dish to SEM room.
c. SEM to determine if gate region is clear. Consult process engineer if there is doubt.
d. Return wafer to petri dish.

6. Gate Recess

a. Prepare GaAs etch in 100 ml beaker
    3 ml phosphoric
    1 ml Hydrogen peroxide
    50 ml room temperature DI H_2O.
b. Place beaker in room temperature bath and cover with watch glass.
c. Using the probe station and a tektronix 576 curve tracer, measure the saturated drain to source current

(I_{ds}) at 5 volts on the 1 μm etch FET in the diagnostic pattern.

d. Record the value of the current observed above.
e. Return wafer to petri dish.
f. Place 1 drop of Microclean in a 100 ml beaker. Add 50 ml of hot DI H_2O.
g. Place near GaAs etch solution.
h. Decant 75 ml of DI H_2O into a 250 ml beaker. Place near GaAs etch.
i. Mount wafer in tri-grip holder.
j. Immerse in microclean 3 seconds.
k. Transfer immediately to GaAs etch solution. Etch for 15 seconds.
l. Transfer to rinse beaker and immerse for 5 seconds.
m. Rinse with running DI for 30 seconds.
n. Dry with N_2
o. Remeasure I_{ds}.
p. Continue steps i through o until $I_{ds} = 60 \pm 5$ mA.

GEORGIA TECH ENGINEERING EXPERIMENT STATION — Schottky Gate Deposition

PROCESS INSTRUCTION FOR GaAs FET — PI-6

SCOPE

To describe the procedure for depositing Schottky gate metallization.

APPLICABLE DOCUMENTS

Contract Number S8-879406-LPY

REQUIREMENTS

1. Equipment

   a. RF sputtering system, Perkin Elmer Model 2400.
   b. Wet chemical fume hood.
   c. Hot plate.

2. Chemicals and Supplies

   a. Ammonium hydroxide
   b. DI H_2O
   c. LN_2
   d. N_2 gas
   e. Beakers, tweezers, tri-grip holder, etc.
   f. Sulfuric acid
   g. Sodium dichromate
   h. glass slides

PROCEDURE

1. Prepare sputtering system
   a. Install Ti/W and Au targets in sputtering system per standard lab procedure.
   b. Press "pump, start".
   c. Fill LN_2 cold trap.

2. Clean Glass slides

   a. Decant 150 ml of sulfuric acid into a 600 ml beaker.
   b. Add 15 grams of sodium dichromate.
   c. Mix and heat to 80 - 100°C.
   d. Mount glass slide in large tri-grip holder
   e. Immerse in chromic solution for 10 seconds
   f. Rinse immediately in hot DI water
   g. Dry thoroughly with opposed jet N_2 blow dry.
   h. Clean second glass slide. Note: one slide should be

smaller in all dimensions than the other.

i. Transport slides to sputtering system and cover with watch glass.
j. Press "vent start"
k. When vented, raise bell jar.
l. Position the small glass slide on table position 4 and check to insure that it is directly under the Ti/W and Au targets when rotated to these positions.
m. Place the larger slide on top of the smaller glass slide.
n. Lower bell jar.
o. Do not start pumping.

3. Clean GaAs

a. Mix 5 ml. of ammonium hydroxide with 50 ml. room temperature DI H_2O.
b. Prepare wetting solution by adding 1 drop microclean to 50 ml DI H_2O.
c. Prepare rinse beaker of hot DI H_2O.
d. Mount wafer in small tri-grip holder.
e. Immerse in wetting solution for 5 sec.
f. Transfer to ammonium hydroxide solution and soak for 10 seconds.
g. Immediately transfer to rinse beaker.
h. After 5 seconds, transfer to running DI H_2O and rinse for 15 seconds.
i. Blow dry with N_2.
j. Place in covered petri dish.
k. Transport to sputtering system.

4. Deposit Schottky Gate Metals

a. Raise bell jar
b. Place wafer in center of glass slide
c. Lower bell jar
d. Press "pump start"
e. Charge LN_2 cold trap
f. Insure that the table is in the raised position.
g. Allow to pump until pressure is $< 2 \times 10^{-7}$ torr.
h. Press "Gas, start".
i. Open Argon valve.
j. Allow to stabilize.
k. Adjust needle valve to obtain a pressure of 8 mTorr.
l. Rotate wafer to position one.
m. Presputter gold target position 3 at 500 watts for 2 minutes. Turn off.
n. Rotate wafer to position 4.
o. Presputter Ti/W target for 10 minutes at 500 watts
p. Turn power down to 50 watts.
q. Rotate wafer under Ti/W target.
r. Sputter deposit Ti/W for 40 minutes.

s. Switch to Au target.
t. Set RF power to 50 watts.
u. Rotate wafer under Au target.
v. Sputter deposit Au for 6 minutes.
w. Turn RF power off.
x. Rotate wafer to position 4.
y. Let cool 3 minutes.
z. Close Argon valve.
aa. Vent system.
bb. Remove wafer and place in covered petri dish.
cc. Press "pump, start".
dd. Turn off RF generator.

SCOPE

To describe the procedures required to pattern the plated gate photoresist.

APPLICABLE DOCUMENTS

Contract Number S8-879406-LPY

REQUIREMENTS

1. Equipment

   a. Photoresist spinner
   b. Glove box for spinner
   c. Oven, fresh air convection, 95°C
   d. Mask aligners, model no. 686B, Kulicke and Soffa and model no. MJB3/HP Karl Suss.
   e. Microscope, 100X to 800X magnification, unitron, model No. TMS-6560.

2. Chemicals

   a. Positive photoresist, Microposit 1350J thinned 3:1.
   b. Developer, Microposit 351
   c. DI water
   d. N_2 gas
   e. Beakers, hold-down wand, tweezers, tri-grip holder. etc.

PROCEDURE

1. Apply Photoresist - Preset Speed - 4000 RPM
   Time - 25 sec

   a. Obtain wafer from PI-6.
   b. Place wafer on vacuum chuck.
   c. Turn on vacuum.
   d. Apply one drop of resist to center of wafer and spin immediately.
   e. Turn off vaccum.
   f. Remove wafer and place in petri dish.
   g. Air dry 10 minutes.

2. Soft Bake

a. Place wafer on filter paper.
b. Insert into soft bake oven.
c. Bake at 95°C for 25 minutes.
d. Remove from oven and allow to cool 3 minutes.

3. Expose and Develop Edges

a. Expose and develop edges as in PI-2.
b. Dry in N_2 gas.
c. Return to petri dish.

4. Align and Expose

a. Install plated gate mask in Suss aligner observing cautions in PI-2.
b. Align mask to previous pattern. Note: Final alignment should be made to the narrow gate layer as observed on the actual FETs.
c. Expose 33 seconds.
d. Remove wafer and place in petri dish.
e. Remove mask and return to storage container.

5. Develop

a. Mix, 1 part developer with 3.5 parts H_2O as in PI-2.
b. Prepare rinse beaker.
c. Place on vacuum hold-down wand.
d. Immerse in developer for 30 seconds.
e. Rinse immediately in DI H_2O beaker for 30 seconds.
f. Rinse an additional 30 seconds in running DI H_2O.
g. Blow dry using dry nitrogen gas.

6. Inspect

Inspect images as in PI-2.

SCOPE

To describe the steps required to selectively electroplate gold for the plated gate.

REQUIREMENTS

1. Equipment

   a. Hot plate, stirrer type.
   b. DC power supply, HP model 721A.
   c. Ammeter, Simpson 270 or equivalent.
   d. Magnetic stirrer, teflon coated.
   e. Surface profiler, tencor alpha step.

2. Chemicals and Supplies

   a. BDT 510 Au Electroplating Solution. Sel Rex Inc.
   b. BDT 510 Brightener.
   c. Test leads.
   d. Ring stand and Clamps.
   e. Platinum Anode, approx. 16 cm^2.
   f. DI H_2O.
   g. Beakers, tweezers, etc.
   h. Glass slide, Au coated, 4.5 cm^2 area of Au coating.
   i. Black wax.
   j. Alligator clip.
   k. Trichloroethylene.

PROCEDURE

1. Prepare Bath

   a. Decant 150 ml. of BDT 510 solution into a 250 ml beaker.
   b. Add 3 ml of brightener.
   c. Place on hot plate and heat to $50^oC \pm 3^oC$.
   d. Insert platinum anode and clamp with tweezers.
   e. Connect positive lead of power supply to anode.
   f. Immerse magnetic stirrer into solution and turn on stirrer.
   g. Turn on power supply.
   h. Set current to 8 mA by touching negative lead to anode. Note: a resistor in series with cathode lead may be required to obtain precise adjustment.
   i. Mask a small area on the glass slide with black wax.
   j. Grasp glass slide with tweezers and clamp with

alligator clip.

k. Connect cathode lead to tweezers.
l. Immerse slide into solution.
m. Adjust current to 8 mA.
n. Plate for 10 minutes.
o. Remove from solution and place in DI H_2O immediately.
p. Rinse in DI and blow dry.
q. Remove wax with trichloroethylene.
r. Measure thickness of deposit with surface profiler.
   Note: thickness should be approximately 8000 angstroms.
s. Inspect color of deposit. If brown, consult process engineer.

2. Plate Wafer

a. Measure the photoresist thickness on the wafer by profiling a FET bond pad region.
b. Clamp the wafer to the non-metallized side of the glass slide with tweezers. Note: the side of the wafer to be plated must be facing outward.
c. Insure that the wafer is clamped in a manner such that good electrical contact is made between the gold layer on the wafer and the tweezers.
d. Connect cathode lead to tweezers.
e. Immerse in plating solution.
f. Clamp tweezers onto ring stand.
g. Adjust current to 8 mA.
h. Plate for 10 minutes.
i. Remove and place in DI H_2O immediately.
j. Rinse thoroughly in hot DI.
k. Blow dry.
l. Measure thickness
   Note: Desired thickness is 8500 $\pm$ 300 angstroms.
m. Replate if necessary, but do not exceed a plating thickness of 1 micron.

GEORGIA TECH ENGINEERING EXPERIMENT STATION Gate Definition

PROCESS INSTRUCTION FOR GaAs FET PI-9

SCOPE

To describe the steps involved in delineating the Schottky barrier plated gate structure.

APPLICABLE DOCUMENT

Contract Number S8-879406-LPY

REQUIREMENTS

1. Equipment

   a. Mask aligner, Kulicke & Soffa, 686B.
   b. Wet chemical fume hood.
   c. Curve tracer, Tektronix 576.
   d. Hot plate.
   e. Sonic cleaner, (low power).
   f. Plasma system, LFE, PDE 301.
   g. Microscope, 100X to 800X magnification.

2. Chemicals and Supplies

   a. Developer solution 1:35 DI H_2O
   b. Techni-strip, Au etchant
   c. Hydrogen peroxide, 30%
   d. Microposit 140 remover, Shipley
   e. DI H_2O
   f. propanol
   g. beakers, tweezers vacuum hold-down wand, tri-grip holder, etc.
   h. magnetic stirrer
   i. ring stand

PROCEDURE

1. Remove top layer of photoresist

   a. Obtain wafer from PI-8.
   b. Expose for 10 sec. with mask aligner.
   c. Develop for 1 minute in std. developer.
   d. Spray develop 30 seconds using 1:1 developer: DI H_2O
   e. Rinse 1 minute.
   f. Blow dry.

2. Etch Au

a. Decant 50 ml of Techni-strip into a 100 ml beaker.
b. Heat to 35°C.
c. Mount wafer into tri-grip holder.
d. Place Au etchant beaker into sonic cleaner.
e. Turn on cleaner.
f. Immerse wafer into solution.
g. Carefully observe wafer surface. When a noticeable color change occurs, remove wafer. A time of 15-20 seconds should be required. Consult proces engineer if visible change is not observed within the time prescribed above.
h. Rinse in DI H_2O (beaker).
i. Blow dry.

3. Inspect

Inspect wafer at high magnification to insure that all traces of undesired gold are removed.

4. Ti/W Etch

a. Decant 50 ml. hydrogen peroxide into a plastic beaker.
b. Immerse water into H_2O_2 with tri-grip holder.
c. Etch for 2 minutes.
d. Rinse with DI H_2O.
e. Immerse in Au etch for 5 seconds.
f. Rinse in DI H_2O.
g. Immerse in H_2O for 10 minutes.
h. Rinse in DI H_2O and blow dry.
i. Expose for 2 seconds.
k. Develop 10 seconds.
l. Immerse in H_2O_2 for 2 minutes.
m. Rinse in DI H_2O
n. Dry with N_2.

5. Inspect

Inspect wafer at high magnification to insure that all traces of Ti/W are removed. Repeat H_2O_2 etch as necessary. Caution: Do not over etch. Perform electrical test as described in PI-10 if necessary.

6. Remove Bottom Layer of Photoresist

a. Decant 50 ml of Microposit 140 Remover into a 100 ml beaker.
b. Place magnetic stirrer in remover.
c. Heat to 50 $\pm$ 5°C.
d. Clamp wafer with tweezers and mount on ring stand.
e. Immerse wafer in remover.
f. Soak for 10 minutes with moderate agitation.

h. Transfer to vacuum hold-down wand and rinse with propanol from wash bottle.
i. Dry with N_2.
j. Insert wafer into plasma system.
k. Strip photoresist for 8 minutes at 350W using an oxygen flow rate of 33 scc/min.
l. Remove from plasma system.
m. Inspect for residue. If residue is present, repeat plasma operation for 3 minutes. Consult process engineer if residue is still present.

SCOPE

To describe procedures for evaluating GaAs FET electrical characteristics.

APPLICABLE DOCUMENT

Contract Number S8-879406-LPY

REQUIREMENTS

1. Equipment

   a. Curve tracer, Tektronix Model 576
   b. Curve tracer camera, Tektronix
   c. Capacitance bridge, Boonton, Model 75D
   d. Probe station
   e. Microscope

2. Chemicals and Supplies

   a. tweezers
   b. test leads

PROCEDURE

1. I-V Characteristics

   a. Set up 576 curve tracer as follows:
      Polarity: NPN
      Step/Offset Polarity: INVERT
      Steps: Depressed
      Step Family: REP
      Rate: NORM
      Emitter Grounded: Step Gen
      Series Resistor: 140 ohms
      Max Peak Volts: 15
      Collector Supply: Fully counterclockwise
      Vertical: 10 mA/div
      Horizontal: 0.5 V/div
      Step Generator Amplitude: 0.5V/step
      Number of Steps: 4 to 6.
   b. Connect source(s) leads to emitter terminal on curve tracer.
   c. Connect drain lead to collector terminal.
   d. Connect gate lead to base terminal.
   e. Obtain wafer from PI-9.

f. Place wafer on probe station and, using a microscope, contact the device under test (DUT) in the following sequence:
   1. Source(s)
   2. Drain
   3. Gate.
g. Increase collector supply voltage until saturated FET characteristic is observed. NOTE: Adjust vertical and horizontal settings as necessary to obtain clear, well spaced signature.
h. Make a photograph of the I-V characteristic using curve tracer camera.
i. Turn collector supply voltage down.
j. Remove photograph and label with device identity.
k. Raise probes in reverse order of step f.

2. Gate to source capacitance

a. Connect source lead(s) to "low" test terminal.
b. Connect gate lead to "high" test terminal.
c. Contact source(s) on GaAs FET with probe.
d. Bring gate probe to close proxmity with gate pad.
e. Set capacitance multiplier to .001.
f. Set capacitance and conductance knobs to zero.
g. Adjust "R/G Zero" and "C Zero" such that null indicator is as low as possible.
h. Contact gate pad.
i. Adjust capacitance and conductance knobs such that null indicator again reads as low as possible.
j. Read capacitance and conductance from dials.
k. Compute correct values by accounting for multipliers.
l. Record values.
m. Raise probes.
n. Remove wafer from chuck and place in covered petri dish.

GEORGIA TECH ENGINEERING EXPERIMENT STATION Via Photoresist

PROCESS INSTRUCTION FOR GaAs FET PI-11

SCOPE

To describe the procedures required to pattern the via photoresist.

APPLICABLE DOCUMENTS

Contract Number S8-879406-LPY

REQUIREMENTS

1. Equipment

   a. Photoresist spinner.
   b. Glove box for spinner.
   c. Oven, fresh air convention, 95°C and 110°C.
   d. Mask aligners, model No. 686B, Kulicke and Soffa and model No. MJB3/HP Karl Suss.
   e. Microscope, 100X to 800X magnification, Unitron, model No. TMS-6560.
   f. Hot plate

2. Chemicals

   a. Positive photoresist, microposit 1350J, Neat
   b. Developer, Microposit 351
   c. DI water
   d. N_2 gas
   e. Beakers, hold-down wand, tweezers, tri-grip holder, etc.

PROCEDURE

1. Clean wafer

   a. Decant 50 ml. of trichloroethylene into 100 ml beaker.
   b. Place on hot plate.
   c. Immerse wafer in vapor for 20 seconds using tri-grip holder.
   d. Rinse with tri from wash bottle
   e. Blow dry.

2. Apply Photoresist - Preset speed 4000 RPM Time - 25 sec

   a. Place wafer on vacuum chuck
   b. Turn on vacuum
   c. Apply one drop of resist to center of wafer and spin

immediately.
d. Turn off vacuum.
e. Remove wafer and place in petri dish.
f. Air dry 10 minutes.

3. Soft Bake

a. Place wafer on filter paper
b. Insert into soft bake oven.
c. Bake at 95°C for 25 minutes
d. Remove from oven and allow to cool 3 minutes

4. Expose and Develop Edges

a. Expose and develop edges as in PI-2.
b. Dry in N_2 gas.
c. Return to petri dish.

5. Align and Expose

a. Install Via mask in Suss aligner observing cautions in PI-2.
b. Align mask to previous pattern. Note: Final alignment should be made to the plated gate layer as observed on the actual FETs.
c. Expose 3 minutes .
d. Remove wafer and place in petri dish.
e. Remove mask and return to storage container.

6. Develop

a. Mix, 1 part developer with 3.5 parts H_2O as in PI-2.
b. Prepare rinse beaker.
c. Place on vacuum hold-down wand.
d. Immerse in developer for 45 seconds.
e. Rinse immediately in DI H_2O beaker for 30 seconds.
f. Rinse an additional 30 seconds in running DI H_2O.
g. Blow dry using dry nitrogen.

7. Inspect

Inspect images as in PI-2.

8. Postbake

a. Place wafer in 110°C oven.
b. Bake for 10 minutes.
c. Remove and return wafer to petri dish.

GEORGIA TECH ENGINEERING EXPERIMENT STATION — Thin Film Deposition

PROCESS INSTRUCTION FOR GaAs FET — PI-12

SCOPE

To describe the procedure for depositing a thin layer of contact metalizaton to facilitate air bridge plating.

APPLICABLE DOCUMENT

Contract Number S8-879406-LPY

REQUIREMENTS

1. Equipment

   a. RF sputtering system, Perkin Elmer Model 2400

2. Chemicals and Supplies

   a. LN_2
   b. glass slides
   c. sulfuric acid
   d. Sodium dichromate
   e. Beakers, tweezers, tri-grip holder etc.

PROCEDURE

1. Prpare sputtering system

   a. Install Ti/W and Au targets in sputtering system per standard lab procedure.
   b. Press "pump, start".
   c. Fill LN_2 cold trap.

2. Clean Glass slides

   a. Decant 150 ml of sulfuric acid into a 600 ml beaker.
   b. Add 15 grams of sodium dichromate.
   c. Mix and heat to 80-100^{o}C.
   d. Mount glass slide in large tri-grip holder.
   e. Immerse in chromic solution for 10 seconds.
   f. Rinse immediately in hot DI water.
   g. Dry thoroughly with opposed jet N_2 blow dry.
   h. Clean second glass slide. Note: one slide should be smaller in all dimensions than the other.
   i. Transport slides to sputtering system and cover with watch glass.
   j. Press "vent, start".

k. When vented, raise bell jar.
l. Position the small glass slide on table position 4 and check to insure that it is directly under the Ti/W and Au targets when rotated to these positions.
m. Place the larger slide on top of the smaller glass slide.

4. Deposit Thin Film Metalization

a. Obtain afer from PI-11
b. Place wafer in center of glass slide
c. Lower bell jar
d. Press "pump, start".
e. Charge LN_2 cold trap.
f. Insure that the table is in the raised position.
g. Allow to pump until pressure is $< 2 \times 10^{-7}$ torr.
h. Press "gas, start".
i. Open Argon valve.
j. Allow to stabilize.
k. Adjust needle valve to obtain a pressure of 8 mtorr.
l. Rotate wafer to position one.
m. Presputter gold target position 3 at 500 watts for 2 minutes. Turn off.
n. Rotate wafer to position 4.
o. Presputter Ti/W target for 10 minutes at 500 watts.
p. Turn power down to 50 watts.
q. Rotate wafer under Ti/W target.
r. Sputter deposit Ti/W for 20 minutes.
s. Switch to Au target.
t. Set power to 50 watts.
u. Rotate wafer under Au target.
v. Sputter deposit Au for 6 minutes.
w. Turn RF power off
x. Rotate wafer to position 4.
y. Let cool 3 minutes.
z. Close Argon valve.
aa. Vent system.
bb. Remove wafer and place in covered petri dish.
cc. Press "pump, start".
dd. Turn off RF generator.

SCOPE

To describe the procedures required to pattern the air bridge photoresist.

APPLICABLE DOCUMENTS

Contract Number S8-879406-LPY

REQUIREMENTS

1. Equipment

   a. Photoresist spinner
   b. Glove box for spinner
   c. Oven, fresh air convection, 95°C
   d. Mask aligners, model No. 686B, Kulicke and Soffa and model No. MJB/HP Karl Suss.
   e. Microscope, 100X to 800X magnification, Unitron, model No. TMS-6560.

2. Chemicals

   a. Positive photoresist, Microposit 1350J neat
   b. Developer, Microposit 351
   c. DI water
   d. $N_2$2 gas
   e. Beakers, hold-down wand, tweezers, tri-grip holder, etc.

PROCEDURE

1. Apply Photoresist - Preset speed - 4000 RPM Time - 25 sec

   a. Obtain wafer from PI-12.
   b. Place wafer on vacuum chuck.
   c. Turn on vacuum.
   d. Apply one drop of resist to center of wafer and spin immediately.
   e. Turn off vacuum.
   f. Remove wafer and place in petri dish.
   g. Air dry 10 minutes.

2. Soft Bake

   a. Place wafer on filter paper.

b. Insert into soft bake oven.
c. Bake at 95°C for 25 minutes.
d. Remove from oven and allow to cool 3 minutes.

3. Expose and Develop Edges

a. Expose and develop edges as PI-2.
b. Dry in N_2 gas.
c. Return to petri dish.

4. Align and Expose

a. Install air bridge mask in Suss aligner observing cautions in PI-2.
b. Align mask to previous pattern. Note: Final alignment should be made to the via layer as observed on the actual FETs.
c. Expose 3 minutes.
d. Remove wafer and place in petri dish.
e. Remove mask and return to storage container.

5. Develop

a. Mix 1 part developer with 3.5 parts H_2O as in PI-2 .
b. Prepare rinse beaker.
c. Place on vacuum hold-down wand.
d. Immerse in developer for 45 seconds.
e. Rinse immediately in DI H_2O beaker for 30 seconds.
f. Rinse an additional 30 seconds in running DI H_2O.
g. Blow dry using dry nitrogen gas.

6. Inspect

Inspect images as in PI-2.

SCOPE

To describe the steps required to selectively electroplate gold for the air bridge.

APPLICABLE DOCUMENT

Contract Number S8-879406-LPY

REQUIREMENTS

1. Equipment

   a. Hot plate, stirrer type
   b. DC power supply, HP model 721A or equivalent
   c. Ammeter, Simpson 270 or equivalent
   d. Magnetic stirrer, Teflon coated
   e. Surface profiler, tencor alpha step

2. Chemicals and Supplies

   a. BDT 510 Au Electroplating Solution.
      Sel Rex Inc.
   b. BDT 510 Brightener
   c. Test leads
   d. Ring stand and clamps
   e. Platinum Anode, Approx. 16 cm^2.
   f. DI H_2O
   g. Beakers, tweezers, etc.
   h. Glass slide, Au coated, 4.5 cm^2 areas of Au coating
   i. Black wax
   j. Alligator clip
   k. Trichloroethylene

PROCEDURE

1. Prepare Bath

   a. Decant 150 ml. of BDT 510 solution into a 250 ml beaker.
   b. Add 3 ml of Brightener.
   c. Place on hot plate and heat to $50^{o}C \pm 3^{o}C$.
   d. Insert platinum anode and clamp with tweezers.
   e. Connect positive lead of power supply to anode.
   f. Immerse magnetic stirrer into solution and turn on stirrer.
   g. Turn on power supply.

h. Set current to 8 mA by touching negative lead to anode. Note: a resistor in series with cathode lead may be required to obtain precise adjustment.
i. Mask a small area on the glass slide with black wax.
j. Grasp glass slide with tweezers and clamp with alligator clip.
k. Connect cathode lead to tweezers.
l. Immerse slide into solution.
m. Adjust current to 8 mA.
n. Plate for 10 minutes.
o. Remove from solution and place in DI H_2O immediately.
p. Rinse in DI and blow dry.
q. Remove wax with trichloroethylene.
r. Measure thickness of deposit with surface profiler. Note: thickness should be approximately 8000 angstroms.
s. Inspect color of deposit. If brown, consult process engineer.

2. Plate Wafer

a. Measure the photoresist thickness on the wafer by profiling a FET bond pad region.
b. Clamp the wafer to the non-metalized side of the glass slide with tweezers. Note: the side of the wafer to be plated must be facing outward.
c. Insure that the wafer is clamped in a manner such that good electrical contact is made between the gold layer on the wafer and the tweezers.
d. Connect cathode lead to tweezers.
e. Immerse in plating solution.
f. Clamp tweezers onto ring stand.
g. Adjust current to 8 mA.
h. Plate for 18 minutes.
i. Remove and place in DI H_2O immediately.
j. Rinse thoroughly in hot DI.
k. Blow dry.
l. Measure thickness, Note: Desired thickness is 1.5 $\pm$ 0.1 microns.
m. Replate if necessary, but do not exceed a plating thickness of 1.7 microns.

SCOPE

To describe the steps involved in thinning the substrate.

APPLICABLE DOCUMENTS

Contract Number S8-879406-LPY

REQUIREMENTS

1. Equipment

   a. Wet chemical fume hood
   b. Mazur lapping machine, model 601
   c. Beuhler polishing machine
   d. Lapping, polishing holder and mandrel
   e. Thickness gauge
   f. Pneumatic pressure fixture
   g. Sonic cleaner
   h. Pyrometer
   i. Hot plate

2. Chemicals and Supplies

   a. Tricholorethylene
   b. 1000 grit lapping compound
   c. Pariffin
   d. Razor blade
   e. Methanol

PROCEDURE

1. Clean Equipment

   a. Clean lapping pedstal and holder with trichloroethylene.
   b. Clean thickness gauge with trichloroethylene.

2. Mount Wafer

   a. Place lapping mandrel on thickness gauge and zero the gauge.
   b. Remove mandrel and place it pedstal side down on a hot plate set a 90^{o}C. Note: Place a sheet of filter paper on the top of the hot plate prior to heating the mandrel.
   c. Monitor the temperature of the mandrel with a pyrometer

placed on the side of the mandrel near the pedstal surface.

d. When the temperature indicated by the pyrometer is 175°F, remove the mandrel.
e. Apply a small amount of parriffin to the mounting surface.
f. Quickly lay the wafer face down in the wax and place a 1" square piece of lens paper over the wafer.
g. Place the mandrel in the pneumatic pressure stand and center under diaphragm. Lower diaphragm holder and turn on the air supply.
h. When cool, release the air pressure and remove the lapping mandrel.

3. Thin the Wafer

a. Remove excess wax with a cotton swab and tricholorethylene.
b. Prepare lapping slurry by sprinkling 1/4 teaspoon of 1000 grit onto glass flat of the lapping fixture and adding deionized water.
c. Measure the wafer thickness using the thickness gauge.
d. Insert mandrel into the lapping fixture holder and set holder into the lapping tray. Move holder around by hand to distribute the grit. Set speed control to 1/2 speed and turn on machine. NOTE: Material removal rate may vary. Check thickness often. Terminate lapping when wafer thickness is ~ 4 mils.
e. Swab edges of wafer with trichloroethylene to remove all traces of grit and excess wax.

4. Remove the wafer

a. Decant 200 ml of DI H_2O into a 250 ml beaker.
b. Heat to > 90°C.
c. Immerse mandrel into hot DI and maintain for approximately 3 minutes.
d. CAREFULLY lift a corner of the wafer with a razor blade.
e. Allow the wafer to fall into the beaker of DI H_2O.
f. Pour off DI H_2O.
g. Remove wafer and place in trigrip holder.
h. Dry with N_2.
i. Remove wax by rinsing in tri.
j. N_2 dry.
k. Return wafer to covered petri dish.
CAUTION: Wafer is now thinner and much more fragile.

GEORGIA TECH ENGINEERING EXPERIMENT STATION — Air Bridge Definition

PROCESS INSTRUCTION FOR GaAs FET — PI-16

SCOPE

To describe the steps involved in delineating the Air Bridge structure.

APPLICABLE DOCUMENT

Contract Number S8-879406-LPY

REQUIREMENTS

1. Equipment

   a. Mask aligner, Kulicke & Soffa, 686B
   b. Wet chemical fume hood.
   c. Hot plate.
   d. Sonic cleaner, (low power)
   e. Plasma system, LPE, PDE 301
   f. Microscope, 100X to 800X magnification

2. Chemicals and Supplies

   a. Developer solution 1:35 DI H_2O
   b. Techni-strip, Au etchant
   c. Hydrogen Peroxide, 30%
   d. Microposit 140 remover, Shipley
   e. DI H_2O
   f. propanol
   g. beakers, tweezers vacuum hold-down wand, tri-grip holder etct.
   h. mangetic stirrer
   i. ring stand

PROCEDURE

CAUTION: <u>Wafer is Fragile</u>

1. Remove top layer of photoresist

   a. Obtain wafer from PI-15
   b. Expose for 10 sec. with mask aligner.
   c. Develop for 1 minute in st. developer
   d. Spray develop 30 seconds using 1:1 developer: DI H_2O.
   e. Rinse 1 minute.
   f. Blow dry.

2. Etch Au

a. Decant 50 ml of Techni-Strip into a 100 ml beaker.
b. Heat to 35°C.
c. Mount wafer into tri-grip holder.
d. Place Au etchant beaker into sonic cleaner.
e. Turn on cleaner
d. Immerse wafer into solution.
f. Carefully observe wafer surface. When a noticeable color change occurs, remove wafer. A time of 15-20 seconds should be required. Consult process engineer if visible change is not observed within the time prescribed above.
g. Rinse in DI H_2O (beaker).
h. Rinse in running DI.
i. Blow dry.

3. Inspect

Inspect wafer at high magnification to insure that all traces of undesired gold are removed.

4. Ti/W Etch

a. Decant 50 ml. hydrogen peroxide into a plastic beaker.
b. Immerse wafer into H_2O_2 with tri-grip holder.
c. Etch for 2 minutes.
d. Rinse with DI H_2O
e. Immerse in Au etch for 5 minutes.
f. Rinse in DI H_2O.
g. Immerse in H_2O_2 for 10 minutes.
h. Rinse in DI H_2O and blow dry.
i. Expose for 2 seconds.
j. Develop 10 seconds.
k. Immerse in H_2O_2 for 2 minutes.
l. Rinse in DI H_2O.
m. Dry with N_2.

5. Inspect

Inspect wafer at high mangification to insure that all traces of Ti/W are removed. Repeat H_2O_2 etch as necessary. Caution: Do not over etch.

6. Remove Bottom Layer of Photoresist

a. Decant 50 ml of Microposit 140 Remover into a 100 ml beaker.
b. Place magnetic stirrer in remover.
c. Heat to 50 + 5°C.
d. Place wafer in tri-grip holder.
e. Immerse wafer in remover.

f. Soak for 10 minutes with moderate agitation.
g. Remove and immediately immerse in propanol.
h. Transfer to vacuum hold-down wand and rinse with propanol from wash bottle.
i. Dry with N_2.
j. Insert wafer into plamsa system.
k. Strip photoresist for 8 minutes at 350W using an oxygen flow rate of 33 sec/min.
l. Remove from plasma system.
m. Inspect for residue. If residue is present, repeat plasma operation for 3 minutes. Consult process engineer if residue is still present.

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GEORGIA TECH ENGINEERING EXPERIMENT STATION Sort

PROCESS INSTRUCTION FOR GaAs FET PI-18

SCOPE

To describe the procedure for sorting discrete GaAs FETs.

APPLICABLE DOCUMENTS

Contract Number S8-879406-LPY

REQUIREMENTS

1. Equipment

   a. Microscope, Stereostart Zoom, AO.
   b. Microscope, 100X to 800X magnification. Unitron, Model No. TMS-6560.

2. Chemicals and Supplies

   a. Plastic dice trays, fluoroware
   b. tweezers
   c. Plastic boxes

PROCEDURE

a. Visually inspect chips with stereo microscope for obvious anomalies.
b. Place visually good chips in dice trays.
c. Place visually bad chips in a properly labeled plastic box.
d. Visually inspect good chips at high magnification using other microscope.
e. Cover dice trays with proper cover and label.